ELECTRONICS

SEMI - CONDUCTOR

→ Band - theory of cond^n

↓

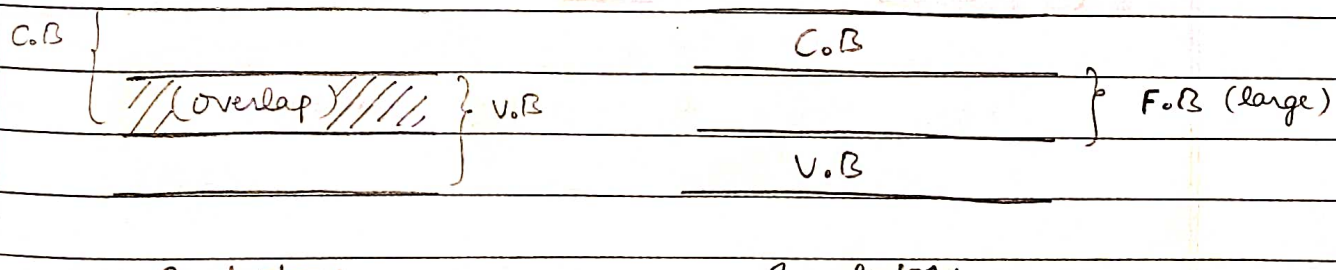
(Range of Energies)

e$^-$ of isolated atoms occupy discrete energy levels. But, when atoms come close, these energy levels are disturbed.

This disturbances cause e$^-$s to occupy a range of energies, called a band.

Bands
- Valence – e$^-$ is associated with atom
- Cond^n – e$^-$ free from atom i.e it can conduct electricity
- Forbidden – Gap b/w Valence & Conduction bands i.e e$^-$ cannot occupy energies in this band

Forbidden band decides the nature of material i.e conductor, insulator or semi-conductor.



Conductors Insulators

C.B

} F.B (small)

V.B

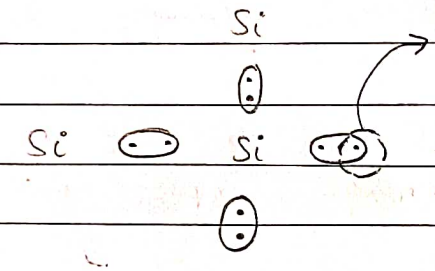
Semiconductors

eg | Si | Ge

F.B | 1.1 eV | 0.7 eV

Si forms bonds with neighbouring Si atoms.

∴ No free e^-



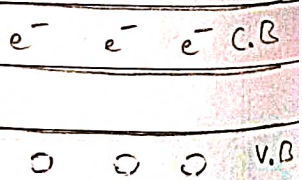
But thermal excitation causes bond to break & e^- jumps from V.B → C.B (Pure / Intrinsic semi-conductor)

∴ Hole created in V.B

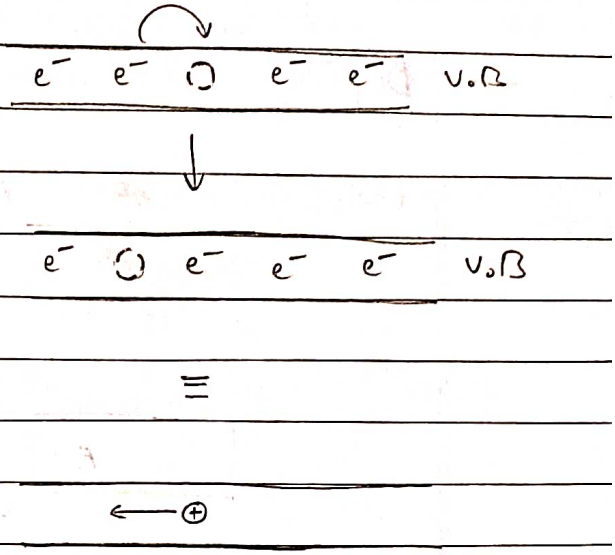
In pure s-cond., intrinsically (# Holes in V.B) = (# e^- in C.B)

⇒ $n_i = N_H = N_e$

(Intrinsic conc. of charge carriers)



→ **Hole as a charge carrier**



On application of $\vec{E}_{ext}$, hole moves toward dirn of $\vec{E}$.
Hence current flows

So, hole behaves as +ve charge

- **Mobility** – Drift speed acq. by charge carrier in unit $\vec{E}$

μ_H → mobility of Hole
μ_e → mobility of e^-

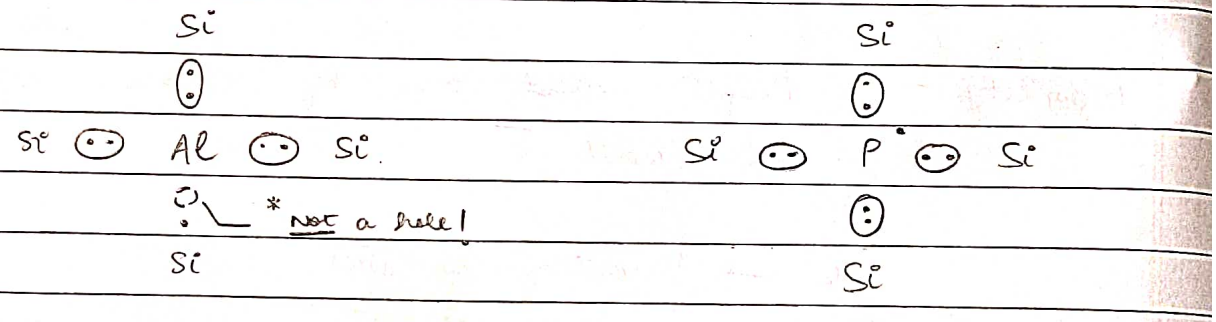
⇒ $\boxed{V_{d_e} = \mu_e E}$ $\boxed{V_{d_H} = \mu_H E}$

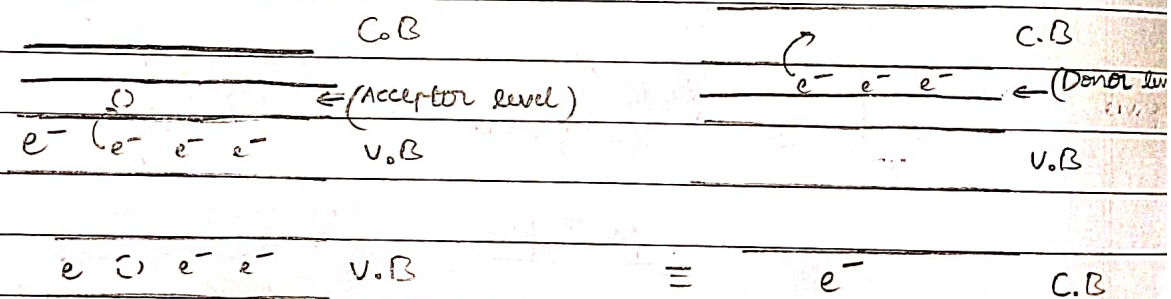
$\mu_e > \mu_H$ (∵ some energy is lost in breaking bound e⁻ for filling the Hole)

→ **Doping** (Extrinsic Semiconductor)

Mixing of impurities in pure semiconductor

- Doping
  - Acceptor Type — 3 valence e⁻s
  - Donor Type — 5 valence e⁻s





≡ e ○ e⁻ e⁻ V.B ≡ e⁻ C.B

p-type s-cond. n-type s-cond.

Majority charge carriers — Holes	Majority — free e⁻
Minority charge carriers — free e⁻	Minority — Holes

$N_H \sim N_A$ $N_e \sim N_D$

NOTE: Hole is formed from where the e⁻ is brought to fill the hole i.e V.B

$$N_H \cdot N_e = N_i^2$$

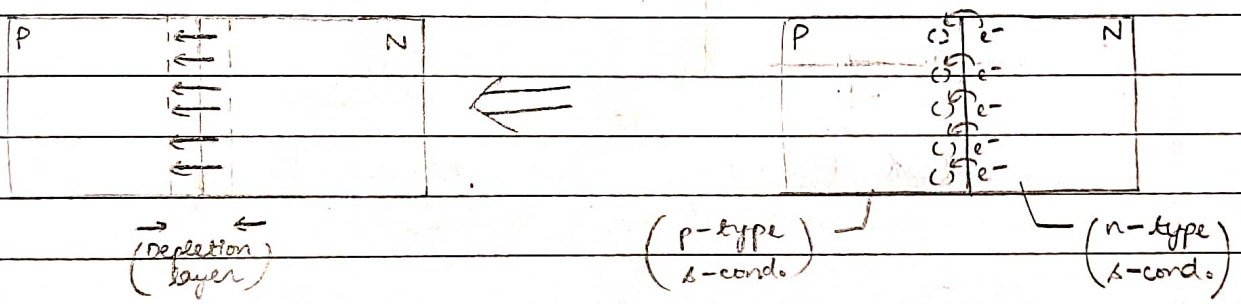
Q. $N_i = 10^{14}/m^3$. Si crystal doped with acceptor type impurity. 1 out of 10^8 Si atoms is displaced by acceptor atom. If Si has 10^{28} atoms/m^3, find N_H & N_e

A. $N_H = N_A = 10^{28-8}/m^3 = 10^{20}/m^3$ $\because N_H \cdot N_e = N_i^2$

$\Rightarrow N_e = 10^{(14)\times 2 - 20}$

$= 10^8/m^3$

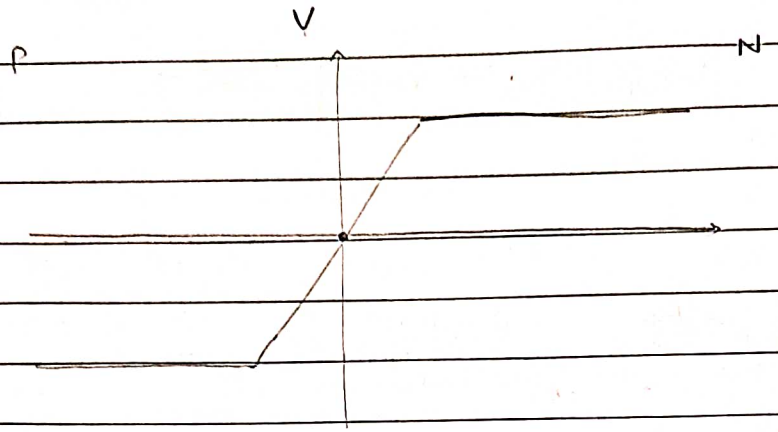
PN JUNCTION DIODE



$\vec{E}$ formed in depletion layer directed from N → P

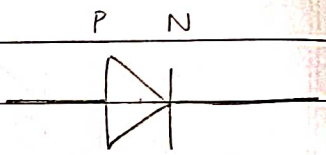
This develops a potential diff. b/w N & P known as barrier pot. diff

Any charge carrier must acq. qV energy to overcome the depletion layer. Hence it prevents dep. layer from growing.

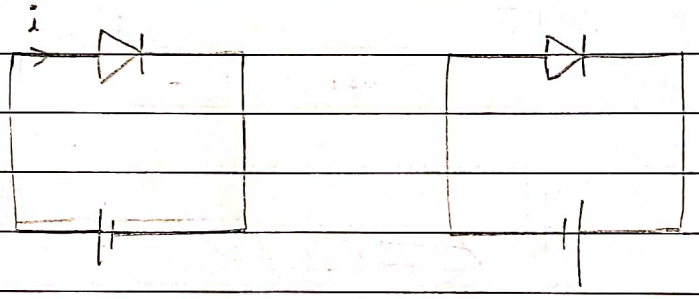


→ Biasing

Connecting PN junction diode to battery is called biasing



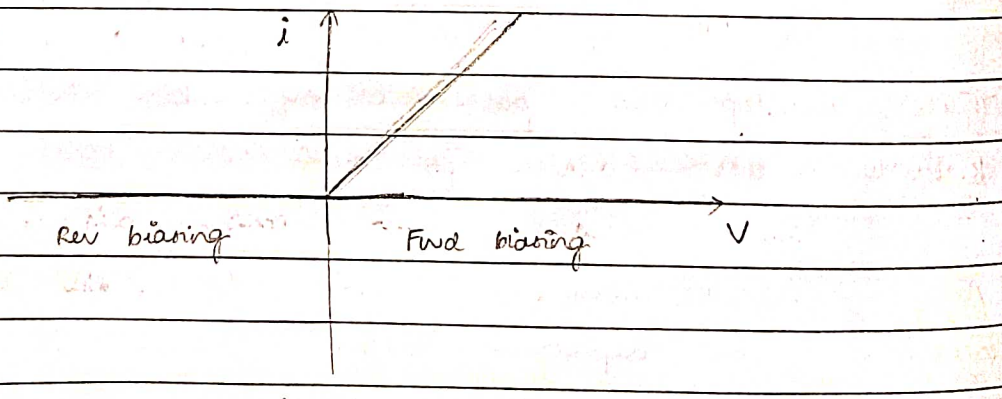
(Electronic symbol for PN diode)



Fwd biasing

Reverse biasing

Ideal PN jn diode allows current to flow in only one dirn i.e fwd.

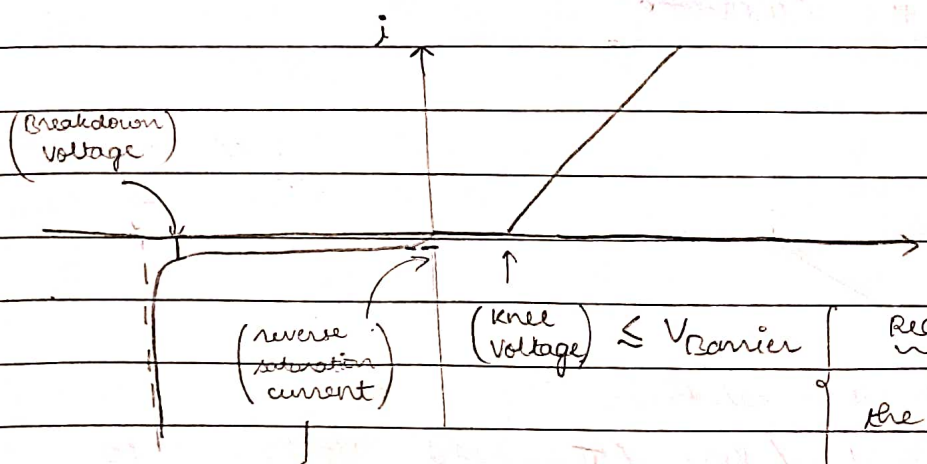


Ideal

Applying Ext (by battery) in a particular bias alters the depletion layer & barrier voltage

Rev → D.L & B.V ↑

Fwd → D.L & B.V ↓



Reason: Applying Ext reduces the size of depletion layer.

Minor charge carriers are able to conduct electricity [e⁻ – P-type] [⊙ – N-type] Actual

size of depletion layer ↑

Breakdown
- Avalanche – (Breaking of bond due to high KE of minority charge carriers accelerated by ext. field)
- Zener – (Breaking of bond due to force applied on bound e⁻ by external field)

Current
- Diffusion – (Movt. of charge carriers towards PN junction).
- Drift – (Movt. of charge carriers away from PN junction due to external field) [Formed at PN junction]

In Fwd biasing → only diffusion current

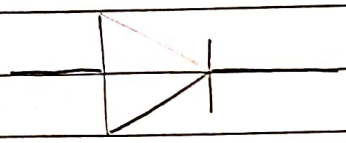
Rev. biasing → both diffusion & drift curren

DIODE IN CIRCUITS

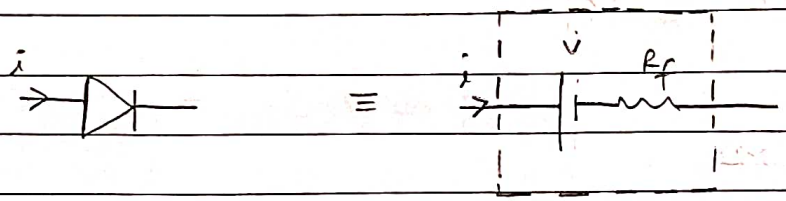
Behaves as

Fwd biased — Wire

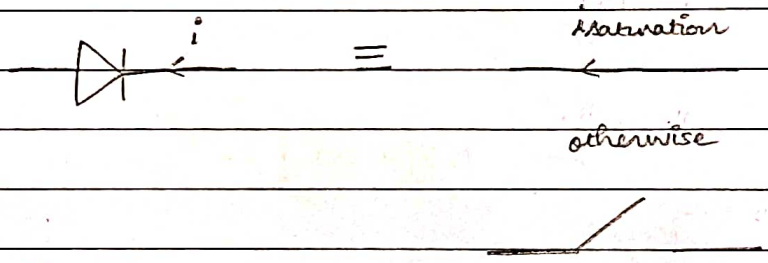
Bwd biased — Open switch



- Fwd biased resistance (R_f) to be considered if gi
- Barrier V / Knee / Threshold Voltage to be considered as a battery if given



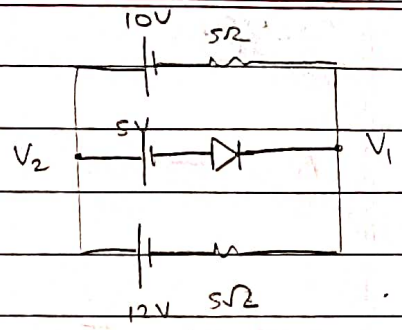
- Reverse saturation current to be considered if given



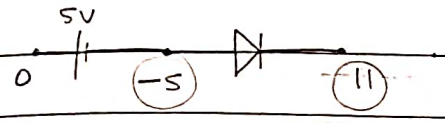
REMARK: To solve circuits, if <u>not</u> evident assume diode to be either fwd or bwd biased.
Proceed as usual. If no contradictions arise, the assumption is correct.

eg

Let's assume the diode is rev. biased



$\Rightarrow \quad V_1 - V_2 = 11$

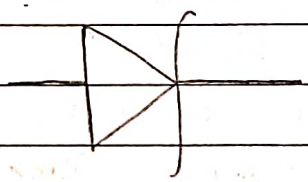


Since $11 > -5$ *

$\Rightarrow$ Diode is rev. biased !

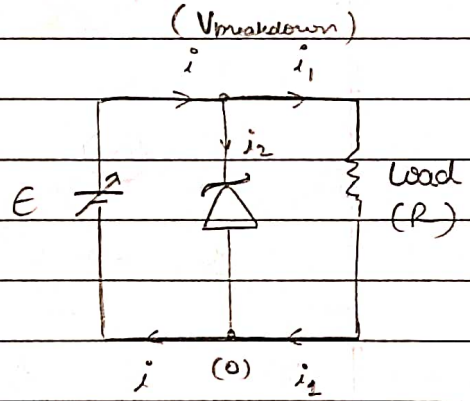
* {Potential across diode to be considered}

→ Zener diode



Always attached bwd biased in circuit

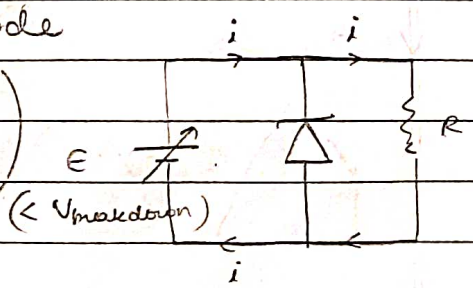
Its breakdown voltage is used to regulate voltage across a load



If $\epsilon > V_{breakdown}$,
it draws current s.t $V_{breakdown}$ maintained across it

Otherwise, acts as regular diode

(open switch in this case since rev. biased)

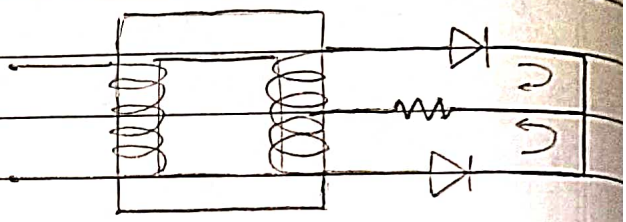


→ Rectifier

AC → DC

• Central Transformer Method

Load in which DC req. attached to centre.

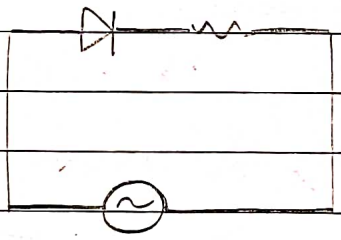


Full-wave rectifier

On one half-cycle of AC, one diode is fwd biased & other is rev biased

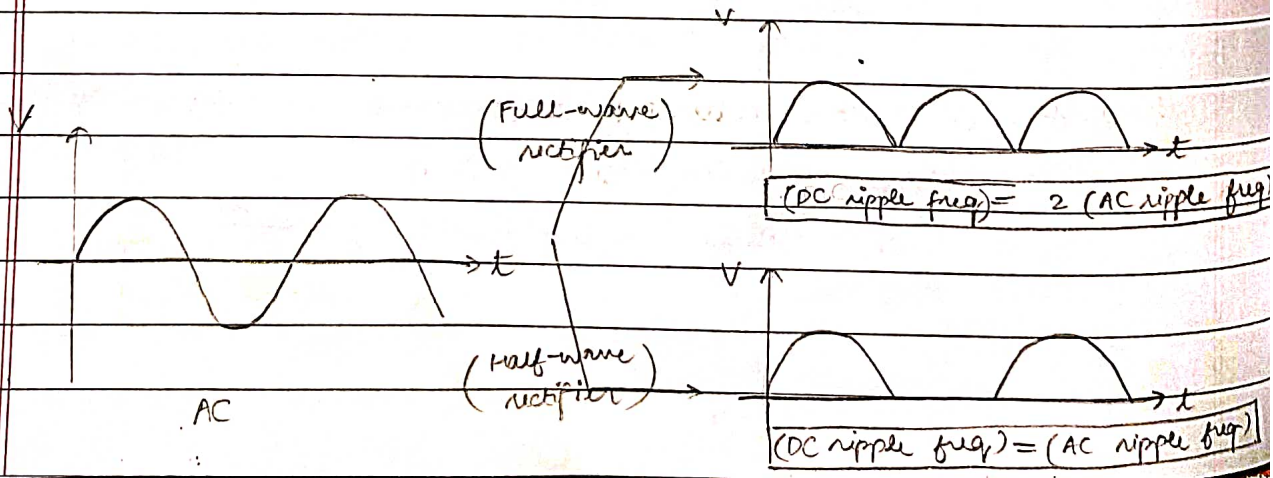
Hence current is maintained in same dirⁿ for load

(Current rectified in full cycle)



Half-wave rectifier

Current only rectified in one of the half-cycles.



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Date
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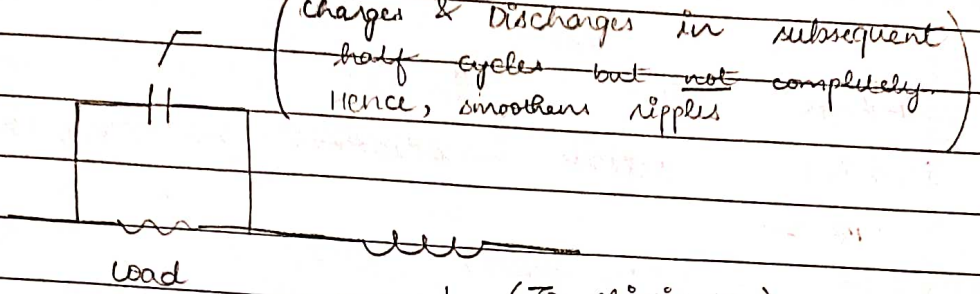
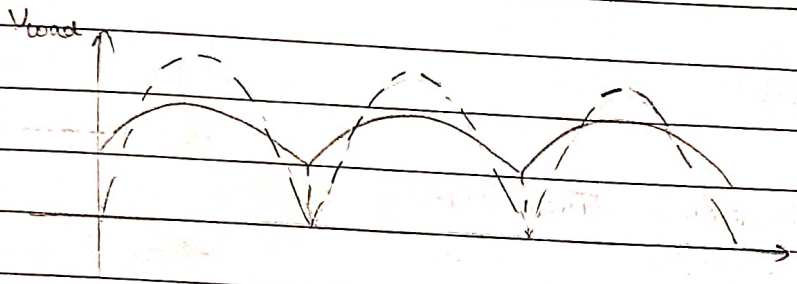
Note: To smoothen D.C ripples, we use Filter Circuit



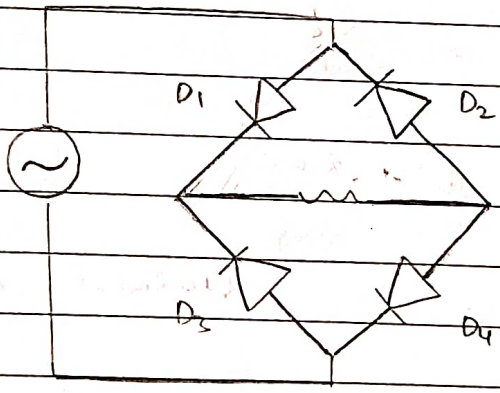
(Charges & Discharges in subsequent ~~half cycles~~ but ~~not~~ completely. Hence, smoothens ripples)

(To eliminate AC component of current)



- Bridge Rectifier

In one half cycle of AC, either D_1 & D_4 or D_2 & D_3 are active.



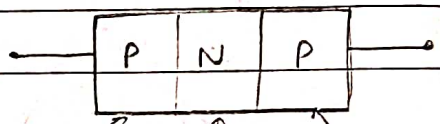
So current is maintained in same dirn for load

→ Light Emitting Diode (LED)

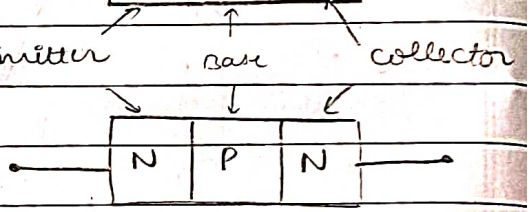
When attached in rev. biased, excites e^- which release radiation on de-excitation

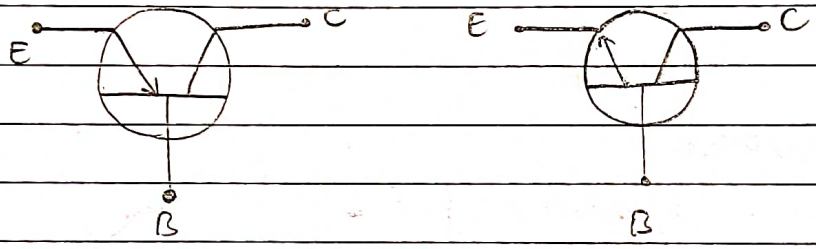
TRANSISTOR

3 terminal device



Bipolar Junction Transistor (BJT)





p-n-p transistor

n-p-n transistor

Electronic symbols

REMARK: Dirⁿ of Arrow shows the dirⁿ of current flowing in Fwd biased E-B Jⁿ

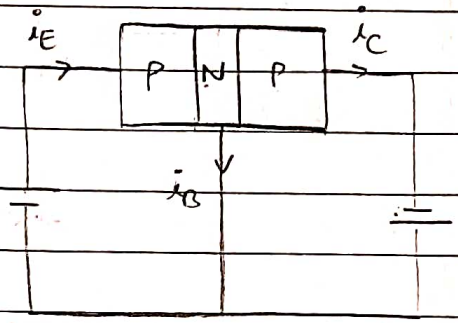
E → B	B → E
(p → n)	(p → n)
⇓	⇓
p-n-p	n-p-n

Physical Characteristics

Base – Thin & low doped
Emitter – Heavy doped
Collector – Moderately doped

$$i_E = i_B + i_C$$

(Input current) (Output current)



Common base config

(Common Base current Gain)

$$\alpha = \frac{i_C}{i_E} \quad \text{for D.C}$$

$$= \frac{\Delta i_C}{\Delta i_E} \quad \text{for A.C}$$

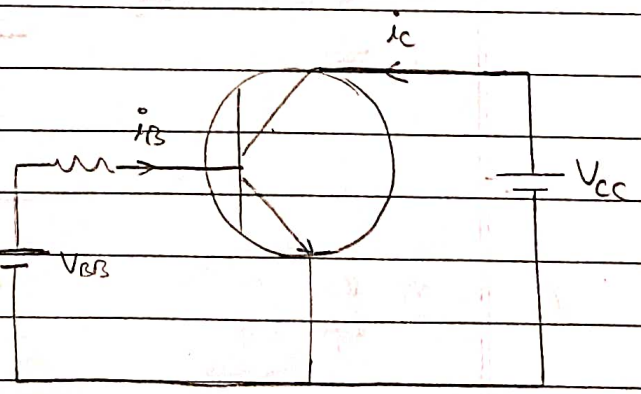
{ α is fixed for a given transistor }

NOTE: Transistor is a current driven device, i.e output current is independant of the battery attached in output circuit

(Common Emitter Current Gain)

$$\beta = \frac{i_C}{i_B} \quad \text{for D.C}$$

$$= \frac{\Delta i_C}{\Delta i_B} \quad \text{for A.C}$$



{ β is fixed for a given transistor }

Common emitter config

NOTE: $\alpha < 1$ & $\beta > 1$

$$\beta = \frac{i_C}{i_B} = \frac{i_C}{i_E - i_C} = \frac{\alpha}{1-\alpha} \Rightarrow \boxed{\beta = \left(\frac{\alpha}{1-\alpha}\right)}$$

OR

$$\boxed{\alpha = \left(\frac{\beta}{1+\beta}\right)}$$

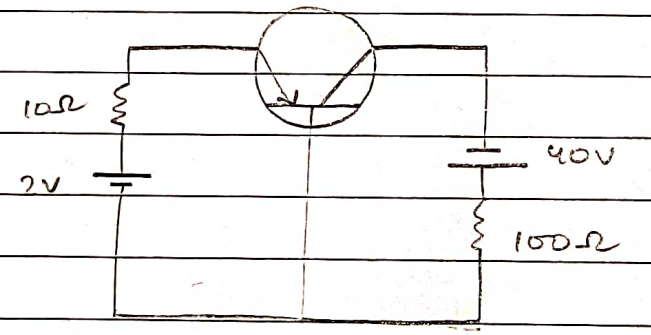
Q In a transistor, only 10% of the charge carriers combine with charge carriers of base. Find β.

A $i_B = \frac{10}{100} i_E \Rightarrow i_B = 0.1\, i_E$

$i_E = i_B + i_C \Rightarrow i_C = 0.9\, i_E \Rightarrow \beta = \frac{i_C}{i_B} = \frac{0.9\, i_E}{0.1\, i_E}$

$= 9$

Q.



$V_{E-B\ jxn} = 0.7\,V$, $\alpha = 0.$

Find i_C, i_B & $V_{C-B\ jxn}$

A. ① KVL on left loop: $2 - 10 i_E - 0.7 \Rightarrow \underline{i_E = 0.13\,A}$

$i_C = \alpha\, i_E = 0.117A$

$i_C + i_B = i_E \Rightarrow \underline{i_B = 0.013}$

② KVL on right loop: $-V_{CB} + 40 - 100\, i_C \Rightarrow \underline{V_{CB} = 28.3\,V}$

NOTE:

1. Here, even if 40 V is changed, i_C remains same since it is only dependent on i_E (through α)
   Instead ΔV_{BC} changes

   If 40 V is changed to less than 4.7 V
   $\Rightarrow \Delta V_{BC} \leq 0 \Rightarrow$ Transistor won't work properly

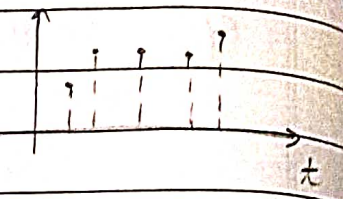
2. This circuit is called Amplifier Circuit as power is getting amplified

31/08/2023

DIGITAL CIRCUITS

Analog – Continuous signal

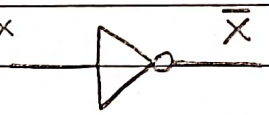
Digital – Discrete signal



We use digital signals since analog signal is more prone to noise during transmission.

- Gate – Digital device having one or many input, but only one output

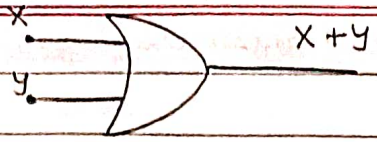
→ Primary Gates

1. NOT (Inverter) – 

X	NOT X ($\overline{X}$)
1	0
0	1

(Truth Table for NOT Gate)

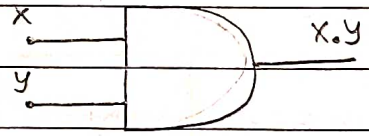
2. OR –



X	Y	X OR Y (X+Y)
0	0	0
0	1	1
1	0	1
1	1	1

(Truth Table for OR Gate)

3. AND –

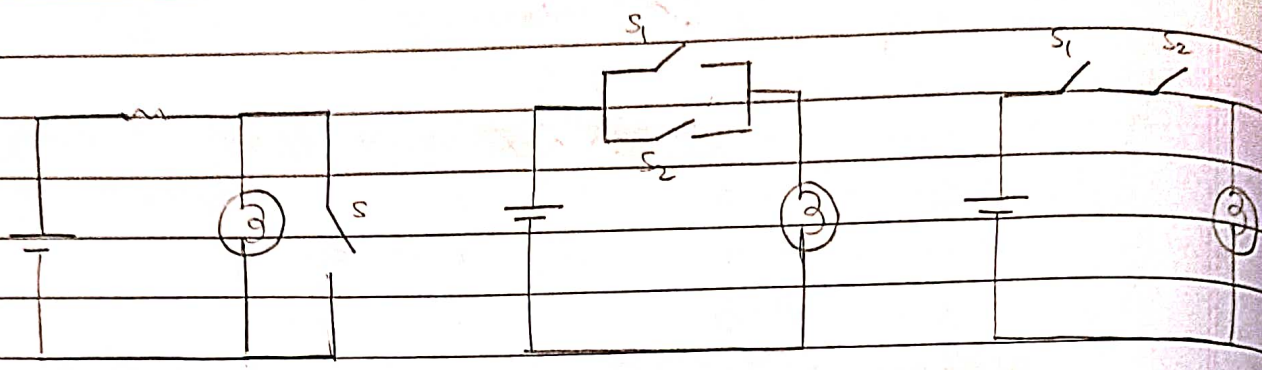


X	Y	X AND Y (X.Y)
0	0	0
0	1	0
1	0	0
1	1	1

(Truth table for AND Gate)

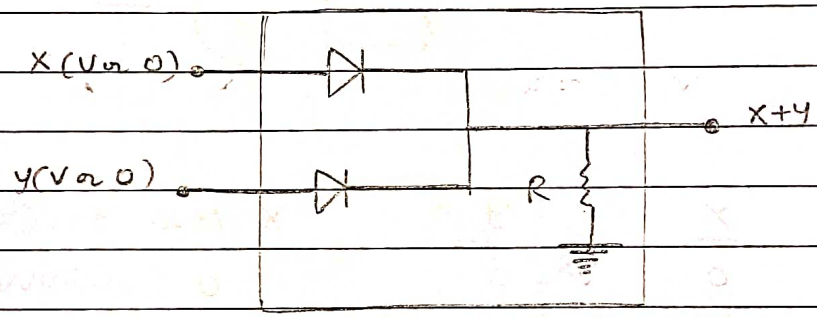
→ Electrical Equivalent

NOT — OR — AND

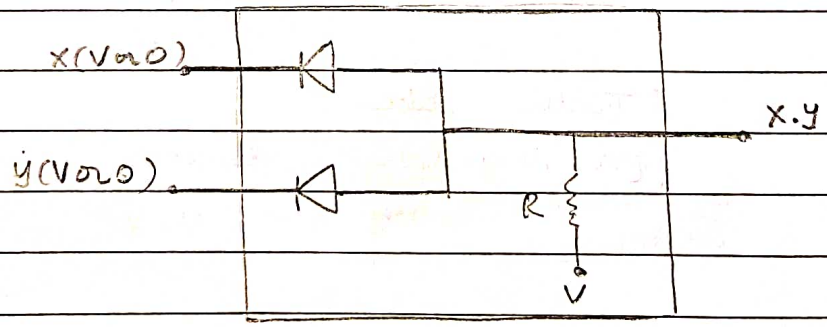


	0	1
Input (Switch) :	open	closed
Output (Bulb) :	Not glowing	glowing

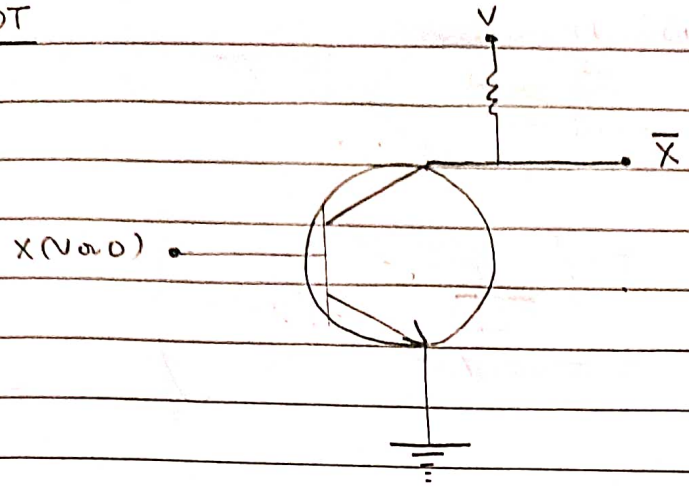
OR



AND



NOT



01/09/2023

→ Boolean Algebra

$X + \overline{X} = 1$ $\quad\quad$ $X.\overline{X} = 0$

$X + 1 = 1$ $\quad\quad$ $X.1 = X$

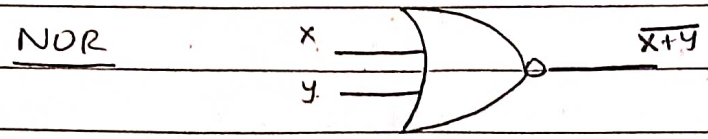
$X + X = X$ $\quad\quad$ $X.X = X$

$X.(Y+Z) = X.Y + X.Z$

De-Morgan's laws – $\overline{X+Y} = \overline{X}.\overline{Y}$

$\overline{X.Y} = \overline{X} + \overline{X}$

NOR



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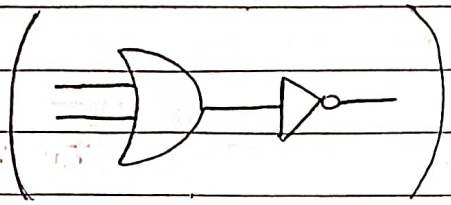
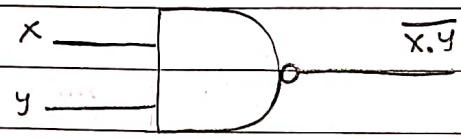


NAND



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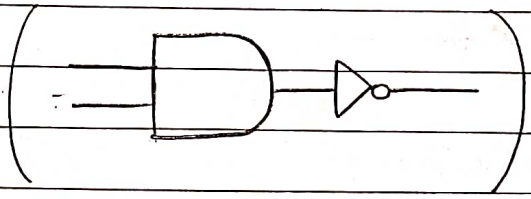
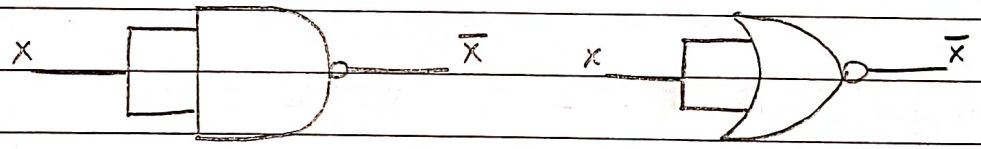
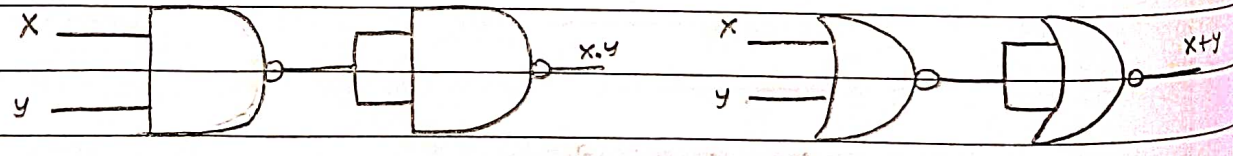


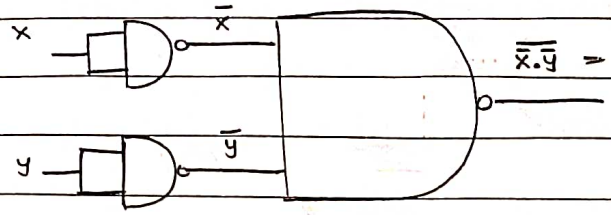
NAND & NOR gates are called universal gates since any gate can be formed using these 2 gates (separately or combined)



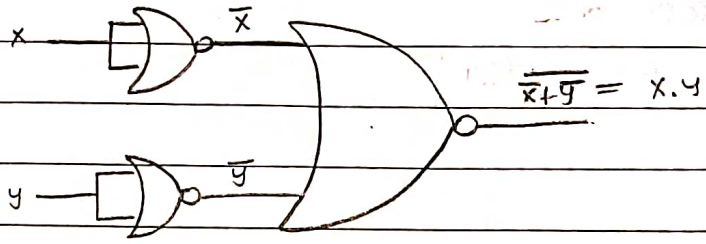
NOT gate using NAND & NOR



AND gate using NAND OR gate using NOR

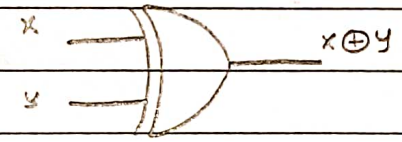


OR gate using NAND



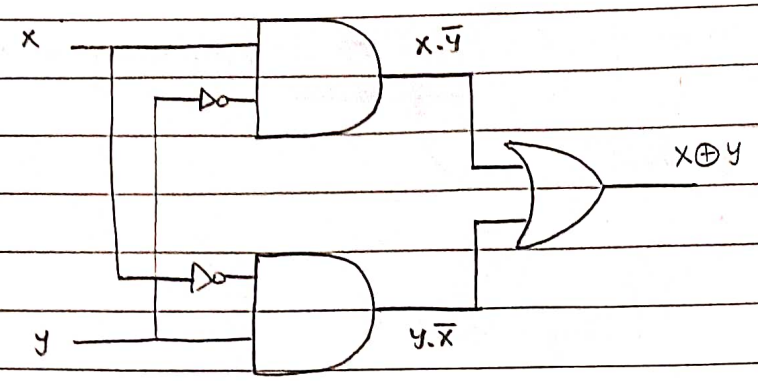
AND gate using NOR

XOR



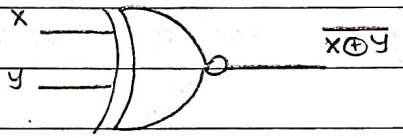
X	Y	$X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

(Truth table for XOR)

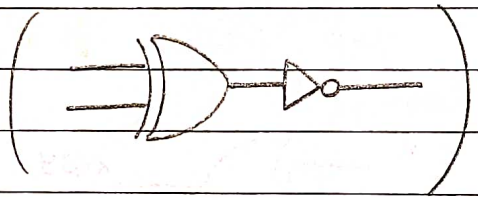


XOR gate
(Half bit adder)

XNOR



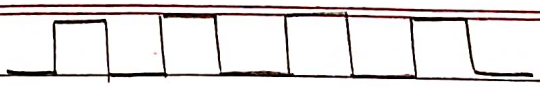
$\equiv$



X	Y	$\overline{X \oplus Y}$
0	0	1
0	1	0
1	0	0
1	1	1

(Truth table for XNOR)

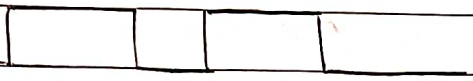
Q. x:



Find the gate.

y:

o:



A. x: 0 1 0 1 0 1 0 1 0

y: 0 1 1 0 0 0 1 1 0

o: 0 0 1 1 0 1 1 0 0 → XOR gate