

IIT Bombay

# Makerspace (MS101)

2024 (Autumn)

**EE-Lecture-10**

**Introduction to Transistors**  
**Using Bipolar Junction Transistor (BJT) and**  
**Metal Oxide Field Effect Transistor (MOSFET) as Switch**

# Transistors: Introduction

A transistor is a semiconductor device with three terminals, used in analog & digital applications. It can be modelled as a 'two-port network', with 'input-dependent output variable'.

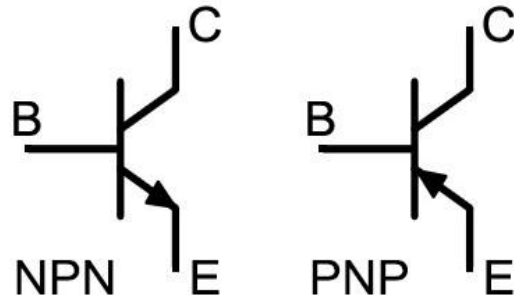
## Commonly used transistors

(a) Bipolar Junction Transistor (BJT)

(b) Metal Oxide Field Effect Transistor (MOSFET)

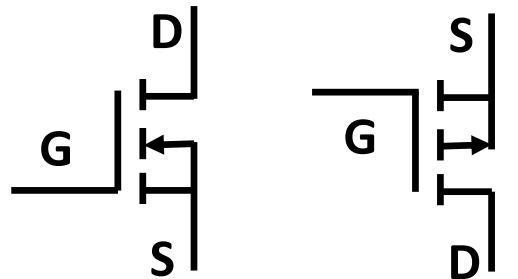
Bipolar Junction Transistor

### Circuit Symbol



B: Base  
C: Collector  
E: Emitter  
 $\beta$ : Current gain

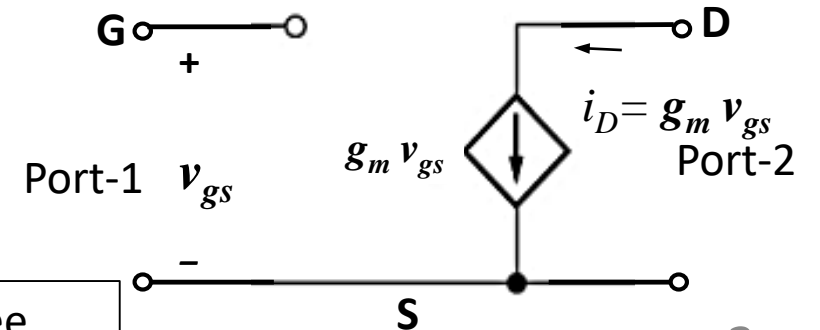
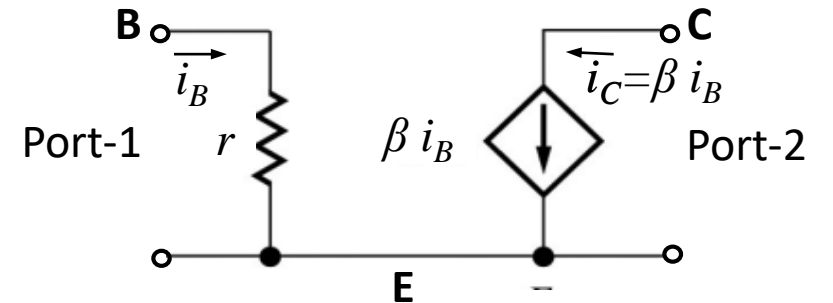
MOSFET  
(Enhancement mode)



G: Gate  
D: Drain  
S: Source  
 $g_m$ : trans-conductance

N-Channel P-Channel

### Simplified Small-Signal Model

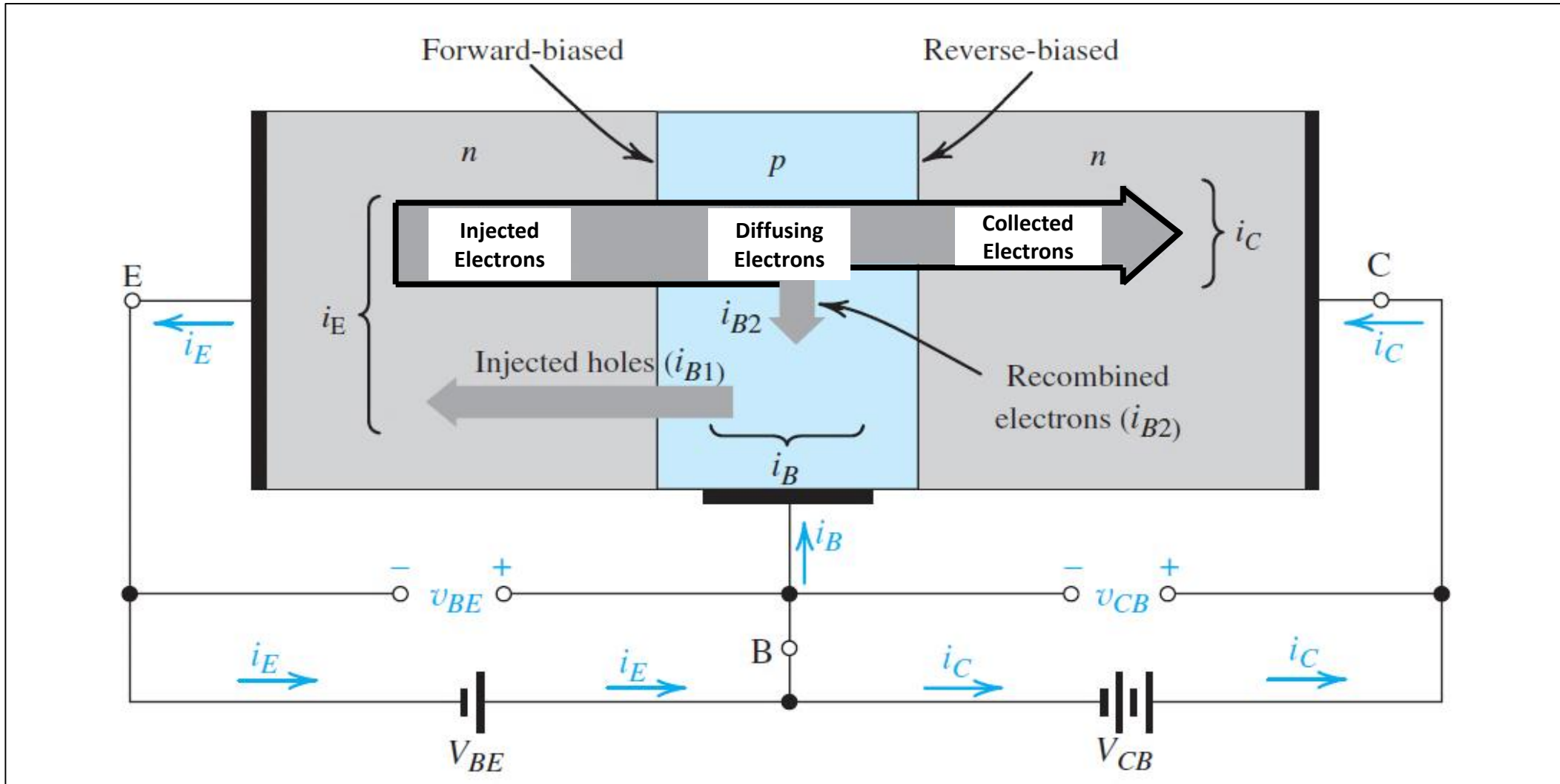


A transistor is operated with one terminal common to both input and output – Three modes of operations for both BJT (CE, CB, CC) and MOSFET (CS, CG, CD)

# Bipolar Junction Transistor (BJT)

<b>Types</b>	NPN, PNP
<b>Terminals</b>	emitter (E), base (B), collector (C)
<b>Controlling quantity</b>	Current-controlled current source: Base Current ( $I_B$ ) controls Collector Current ( $I_C$ ).
BJTs have lower input resistance ( $\approx 10\text{ k}\Omega$ to $1\text{ M}\Omega$ in common-emitter mode) and hence consume more power from the input signal source than MOSFETs.	

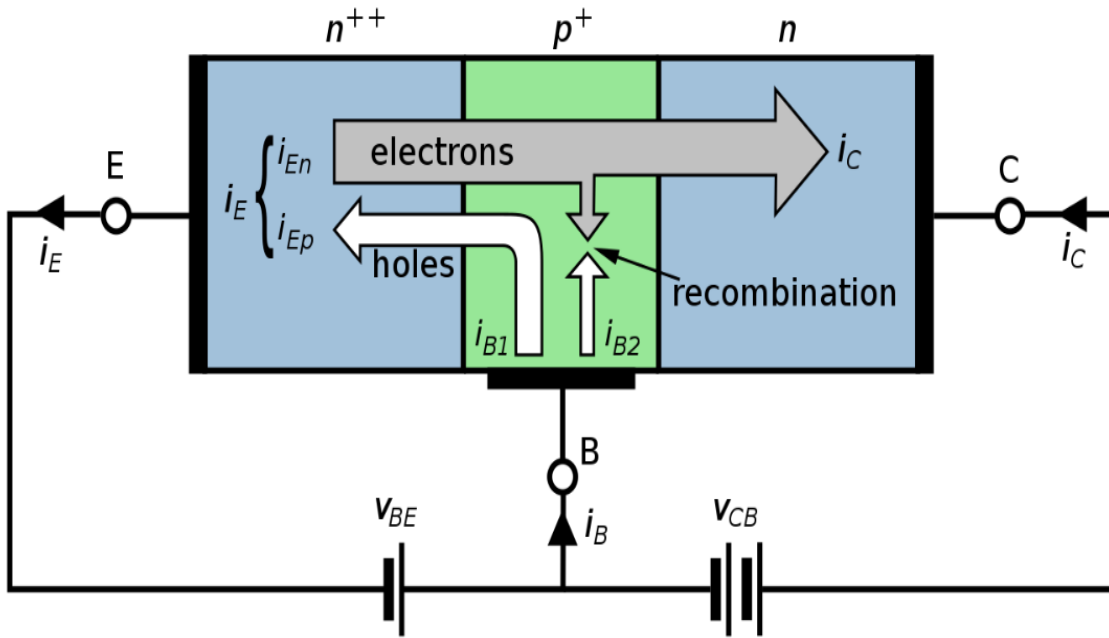
# Bipolar Junction Transistor Operation



**NPN transistor biased in active mode (BE junction: forward biased , BC junction: reversed biased)**

Source: Fig 6.3:-Sedra A S, Smith K C, "Microelectronic Circuits", Oxford University Press, 7Ed. ISBN: 9780199339136

# BJT Operation



## Current relations

KCL:  $I_E = I_B + I_C$

Transistor action

$$\Delta I_C = \alpha \Delta I_E \quad (\alpha \approx 0.90 - 0.99)$$

$$\Delta I_C = \beta \Delta I_B$$

$I_C = \beta I_B$  is used as an approximate relation.

## Cricket analogy

- The emitter is the bowler who shoots balls (electrons) toward the base.
- The base is the batsman, a tail-ender who swings away but connects with only 1-2% of the incoming balls (electrons).
- Most of the balls (electrons) are collected by the wicketkeeper.

## Relation between $\alpha$ & $\beta$

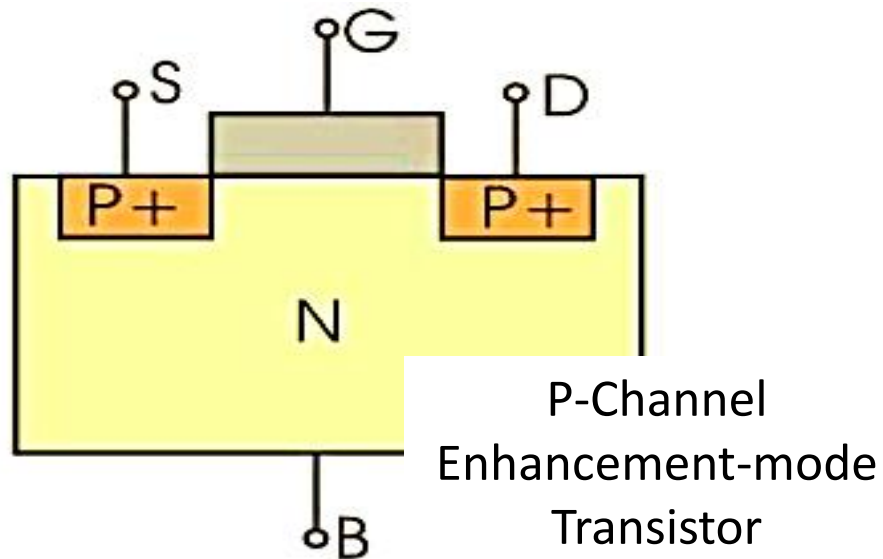
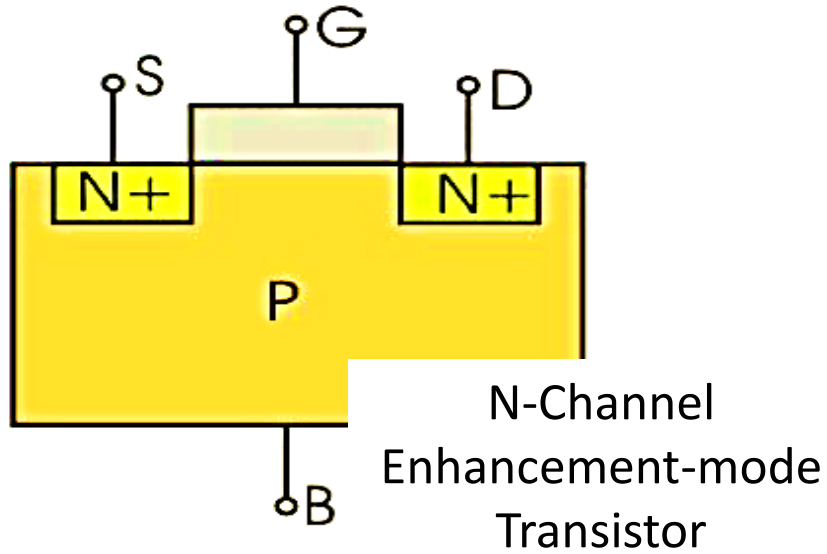
$$\Delta I_E = \Delta I_B + \Delta I_C \Rightarrow \Delta I_B = \Delta I_E - \Delta I_C = (1/\alpha - 1) \Delta I_C$$

$$\Rightarrow \Delta I_C = \alpha / (1 - \alpha) \Delta I_B = \beta \Delta I_B$$

$$\Rightarrow \beta = \alpha / (1 - \alpha)$$

Example:  $\alpha = 0.98 \Rightarrow \beta = 0.98 / 0.02 = 49$

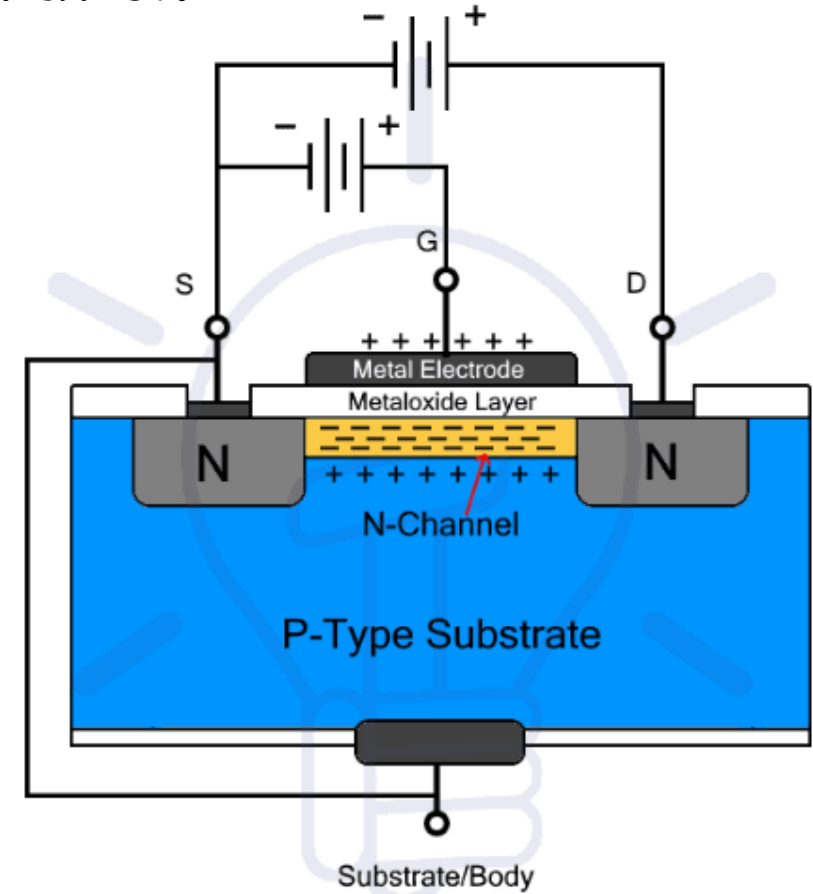
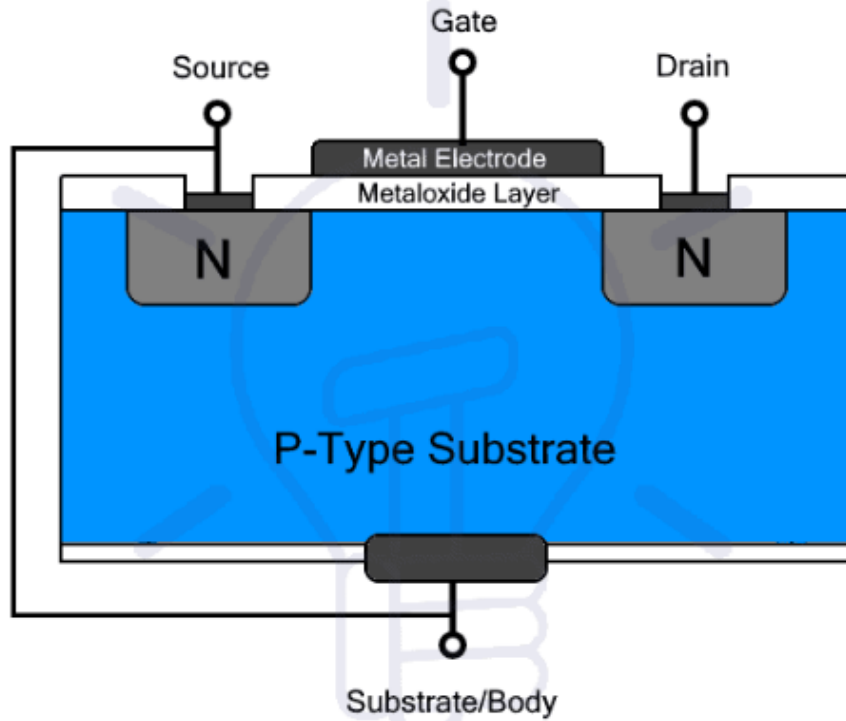
# MOSFETs: Introduction



**Types: N-channel & P-channel, fabricated in enhancement-mode for digital circuits**

Types	N-channel enhancement-mode P-channel enhancement-mode
Terminals	source (S), drain (D), gate (G), substrate or body or bulk.
Controlling quantity	Voltage-controlled current source device: Gate-Source voltage ( $V_{GS}$ ) controls drain to source current ( $I_{DS}$ )
MOSFETs have high input impedance (10 M $\Omega$ to 100 M $\Omega$ ) and hence consume less power from the input signal source than BJTs.	

# N-Channel Enhancement-mode MOSFET Operation



## Device ON / OFF operation

ON: Low resistance for drain-source current flow.  
 OFF: Very high resistance for drain-source current flow.

**Enhancement mode:** No channel is available at  $V_{GS} = 0$ . The channel is formed for  $V_{GS}$  above the threshold voltage  $V_T$  (+ve for N-channel).

MOSFET Type	Condition for Switching
N-channel Enhancement	OFF for $V_{GS} < V_T$ ( 0.6 to 1 V )
P-channel Enhancement	OFF for $V_{GS} > V_T$ ( -1.0 to 0.6 V )

Source: <https://www.electricaltechnology.org/2021/06/mosfet.html>

# Commercially Available Transistor Packages

**TO-92**  
 2SA733  
 2SA934  
 2SC945  
 2SC1571  
 2SC1674  
 2SC1675  
 2SC1730  
 2SC1973

**TO-92L**  
 2SB525  
 2SC2086  
 2SC2538  
 2SD355

**TO-126 (TO-225AA)**  
 2SA1282  
 2SC1906  
 2SC2320  
 2SD471

**TO-220**  
 2SA473  
 2SA1012  
 2SC1306  
 2SC1307  
 2SC1678  
 2SC1969  
 2SC2166  
 2SC2312

**TO-3P(N) (MT-100)**

**TO-3P(L) (TO-247)**

**TO-3 (TO-204AA)**  
 2N6328  
 ECG181  
 NTE181  
 SK9134

**MT-200**

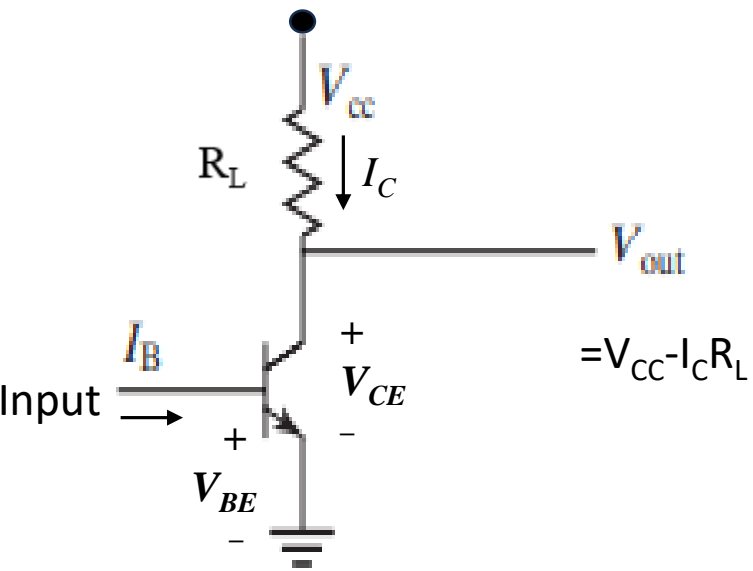
**TO-66 (baby TO-3) (TO-213AA)**

**TO-202**

**TO-39**



# Switching Characteristics of BJT (on $V_{CE}-I_C$ Plane)



BJT is switched ON / OFF by changing the base current  $I_B$ .

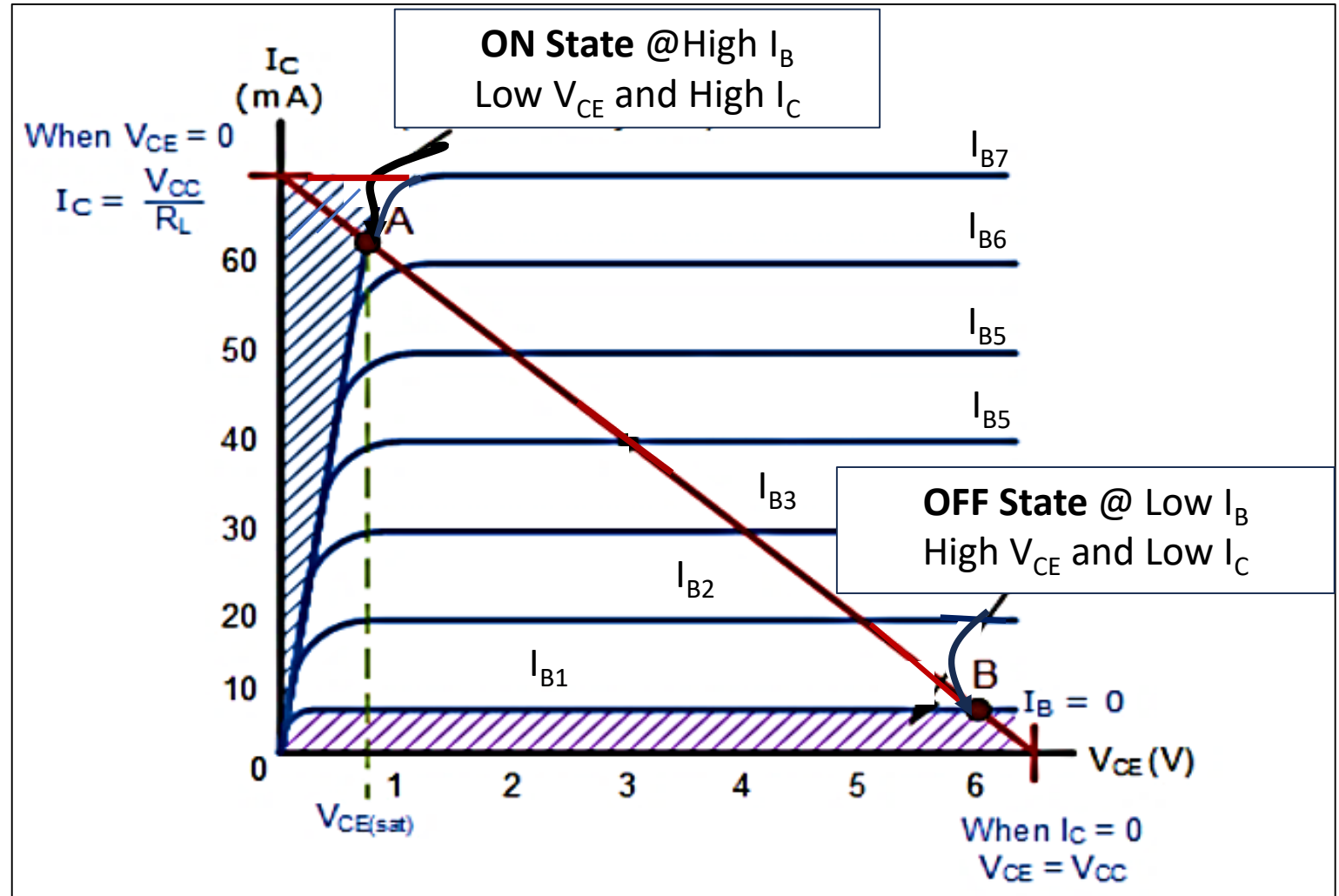
OFF:  $V_{BE} < V_\gamma$ . ( $V_\gamma \approx 0.5 \text{ V}$ )  
 $I_B \approx 0$ .  $V_{CE} \approx V_{CC}$ .  $I_C \approx 0$ .

Heavily ON:  $I_B > I_C / \beta$ .

$V_{BE} = V_{BES}$ .  $V_{CE} = V_{CES}$ .

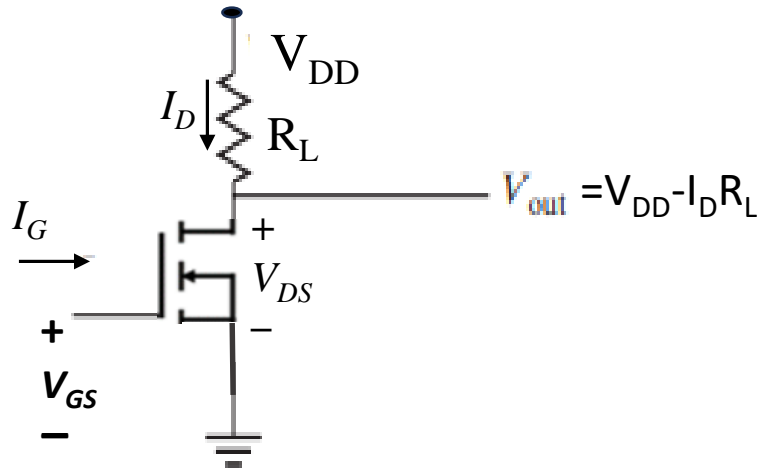
$I_C = (V_{CC} - V_{CES}) / R_L$

( $V_{BES} \approx 0.8 \text{ V}$ .  $V_{CES} \approx 0.2 \text{ V}$ )



Typical ' $V_{CE} - I_C$ ' characteristics for BJT (base currents:  $I_{B1} < I_{B2} < I_{B3} < I_{B4} < I_{B5} < I_{B6} < I_{B7}$ ). Operating points for switching action: A (on) & B (off).

# Switching Characteristics of N-Channel Enhancement-Mode MOSFET (on $V_{DS}-I_D$ Plane)

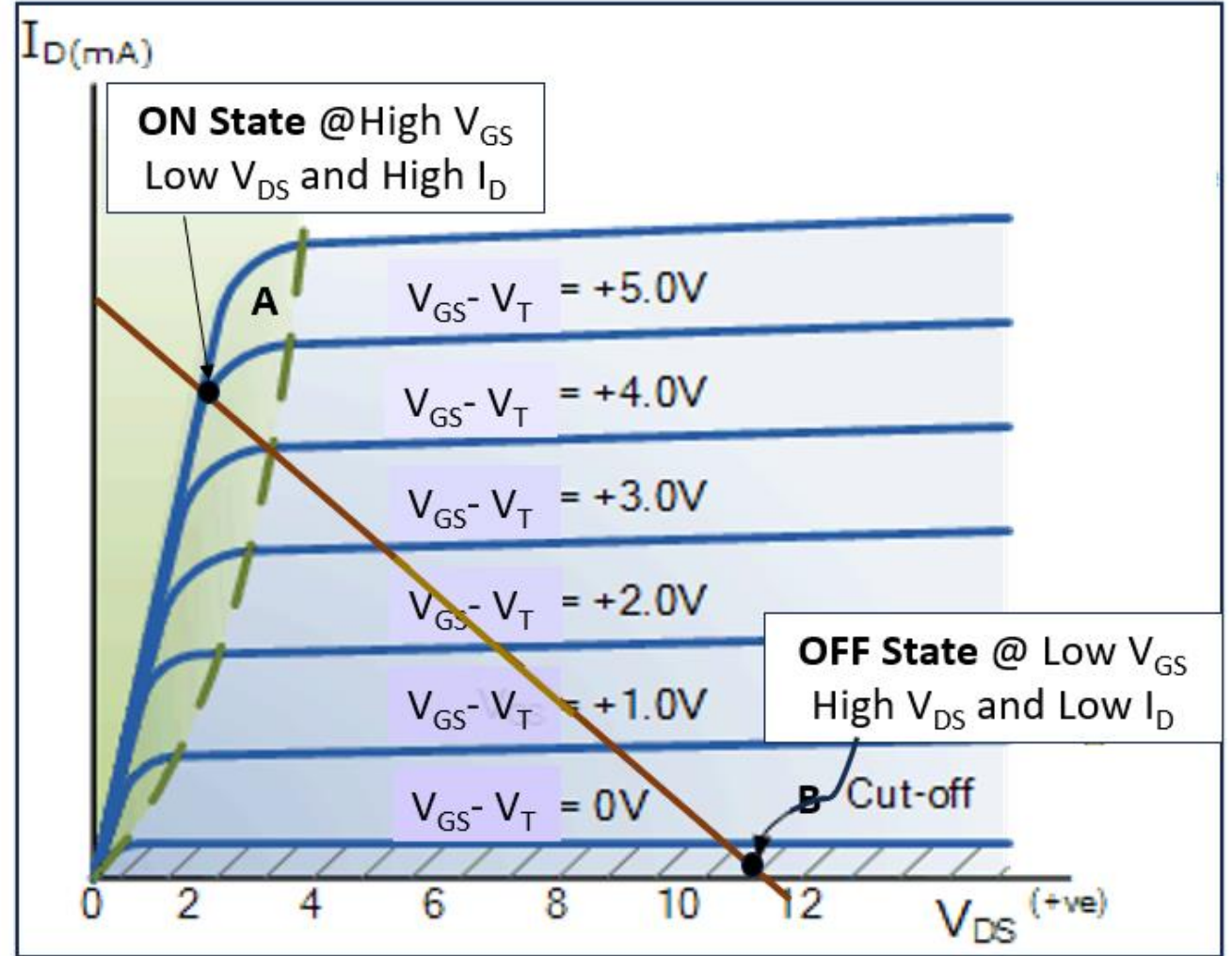


- Enhancement MOSFET starts conducting when the drain-source channel is formed.
- N-Channel MOSFET: N-channel is formed.
- $V_T$  is the minimum value of  $V_{GS}$  for the channel formation.  $V_{GS} > V_T$  for MOSFET to be ON. Channel resistance decreases as  $V_{GS}$  increases further.

OFF:  $V_{GS} < V_T$ .  $I_G \approx 0$ .  $I_D \approx 0$ .  $V_{DS} \approx V_{DD}$

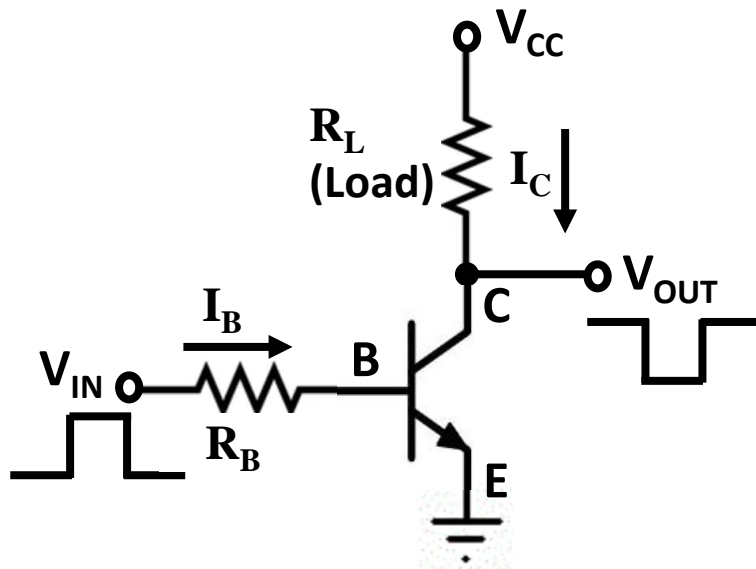
ON:  $V_{GS} > V_T + \text{a few V}$ .

$I_G \approx 0$ .  $V_{DS} \approx 0$ .  $I_D \approx V_{DD} / R_L$ .



Typical ' $V_{DS}-I_D$ ' characteristics for N channel Enhancement mode MOSFET  
A & B: operating points for switching action

# BJT & MOSFET Switching with $V_{in}$ as Control Input

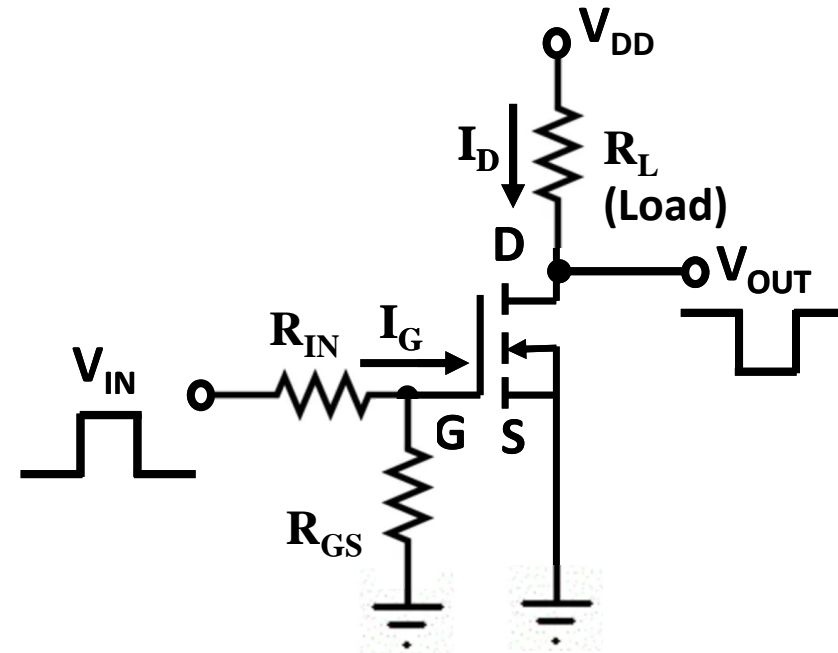


Switch circuit using NPN BJT & control input  $V_{in}$ .

$R_B$  is for limiting  $I_B$ .

OFF:  $I_B \approx 0$ .

ON:  $I_B > I_C/\beta$ .



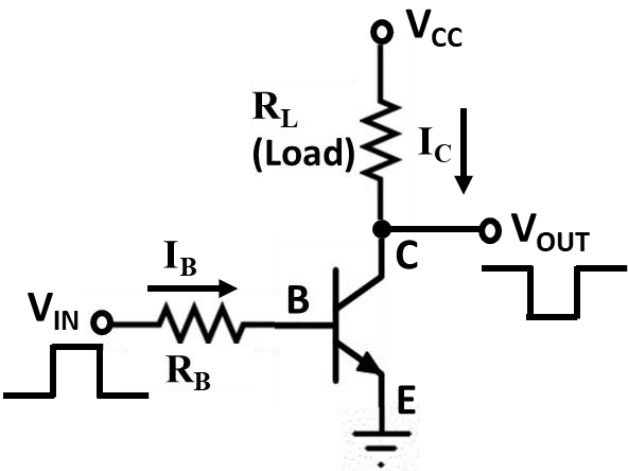
Switch circuit using N-Channel MOSFET & control input  $V_{in}$ .

$R_{in}$  and  $R_{GS}$  are for voltage attenuation, if  $V_{in}$ -peak is large.

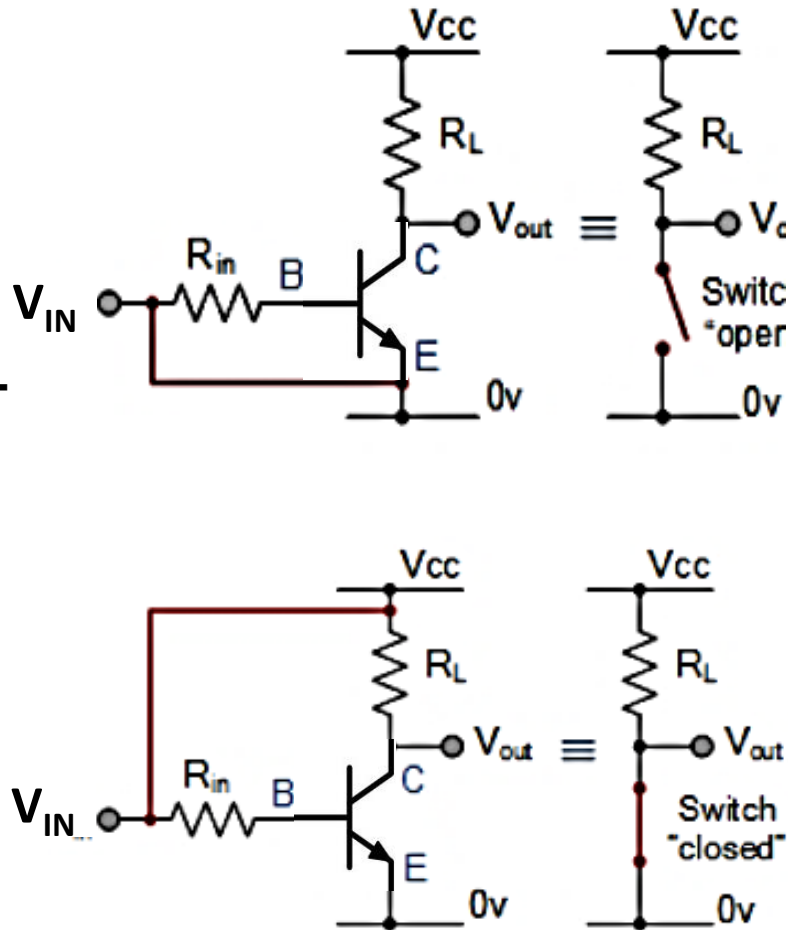
OFF:  $V_{GS} < V_T$ .

ON:  $V_{GS} > V_T + \text{a few V}$ .

# BJT Switching Operation



BJT (NPN) circuit with control input  $V_{IN}$  (binary levels: 0,  $V_{CC}$ ).



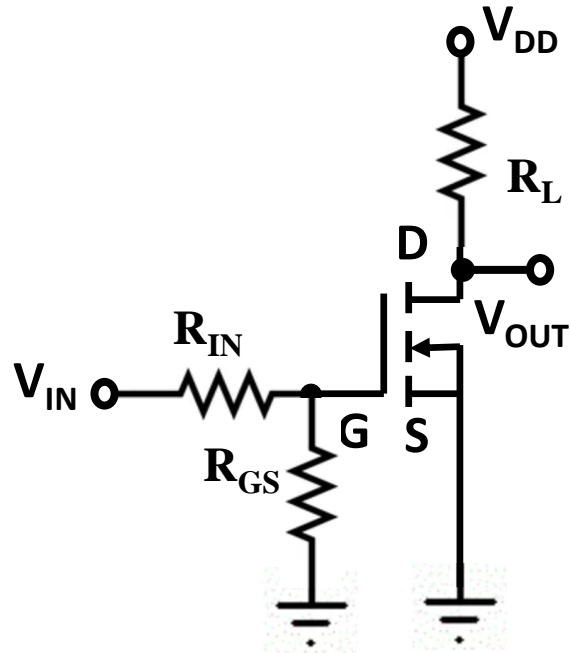
(a)  $V_{IN} = 0$

- $V_{BE} = 0 < 0.5 \text{ V}$ .
- BJT operates as open switch.  
 $I_B \approx 0$ .  $V_{CE} \approx V_{CC}$ .  $I_C \approx 0$ .
- BE junction is not forward biased. BC junction is reverse biased.

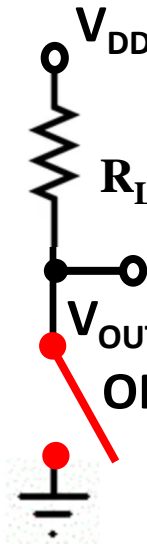
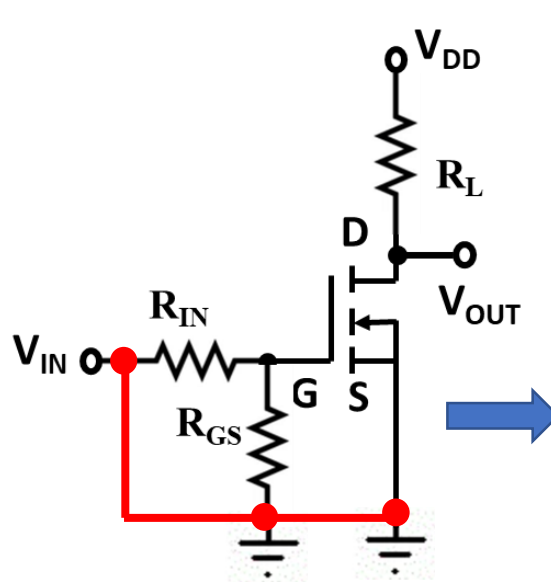
(b)  $V_{IN} = V_{CC}$

- BE junction is forward biased, with  $I_B$  limited by  $R_B$ , with  $V_{BE}$  reaching its saturation value  $V_{BES} (\approx 0.8 \text{ V})$ . Collector voltage drops until BC junction gets forward biased with  $V_{BE}$  reaching its saturation value  $V_{CES} (\approx 0.2 \text{ V})$ .
- BJT operates as closed switch.
- $V_{BE} = 0.8 \text{ V}$ .  $V_{out} = V_{CES} = 0.2 \text{ V}$ .  
 $I_B = (V_{CC} - 0.8) / R_B$ .  
 $I_C = (V_{CC} - V_{CES}) / R_L$ .

# MOSFET Switching Operation



MOSFET (N-channel) circuit with control input  $V_{IN}$  (binary levels: 0,  $V_{DD}$ ). Usually  $R_{in}$  is short and  $R_{GS}$  is open

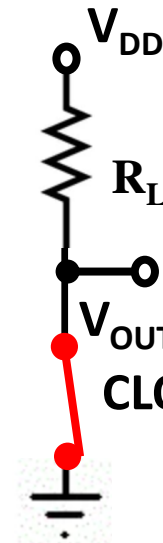
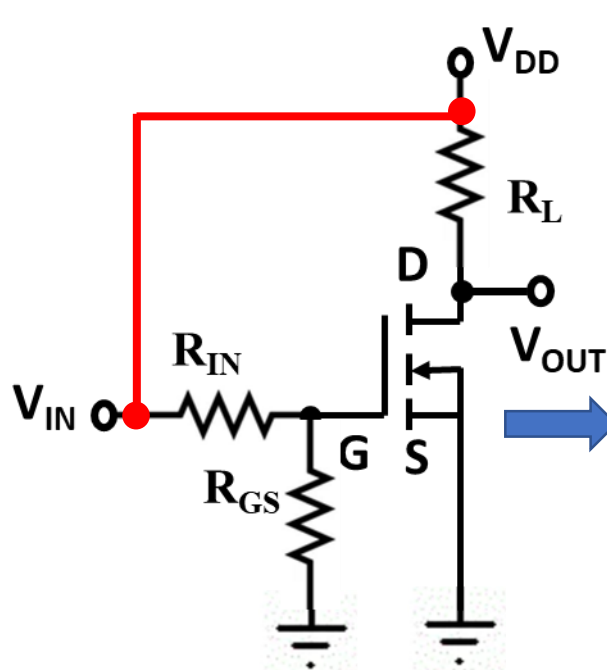


Let  $V_{DD} = 12\text{ V}$ ,  $V_T = 2\text{ V}$ ,  $R_{IN} = 0$ ,  $R_{GS} = \infty$ .

(a)  $V_{in} = 0$

- $V_{GS} = 0 < V_T$ .
- MOSFET operates as open switch.

$I_G \approx 0$ .  $V_{DS} \approx V_{DD}$ .  $I_D \approx 0$ .

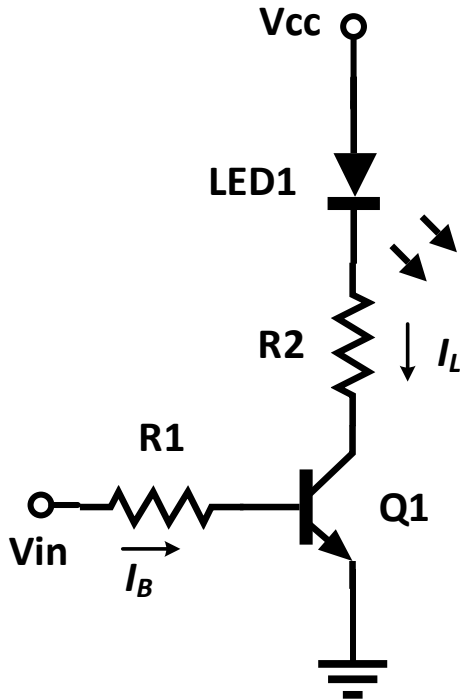


(b)  $V_{in} = V_{DD}$

- $V_{GS} = 12\text{ V} > V_T$ .
- MOSFET operates as closed switch.

$I_G \approx 0$ .  $V_{DS} \approx 0$ .  $I_D = V_{DD}/R_L$ .

**NPN  
Switch for  
Load  
Connected  
to +ve  
Supply End**



$V_{CC} = 5\text{ V}$ .  $V_{in} : 0$  (LED off),  $5\text{ V}$  (LED on).  $\beta > 50$ .  
 $I_L$  for full brightness =  $10\text{ mA}$ . LED drop =  $2\text{ V}$ .

$$I_L = [V_{CC} - V_{LED} - V_{CES}] / R_2 = [5 - 2 - 0.2] / R_2 > 10\text{ mA}$$

$$\Rightarrow R_2 < 2.8 / 10\text{ k}\Omega = 280\ \Omega.$$

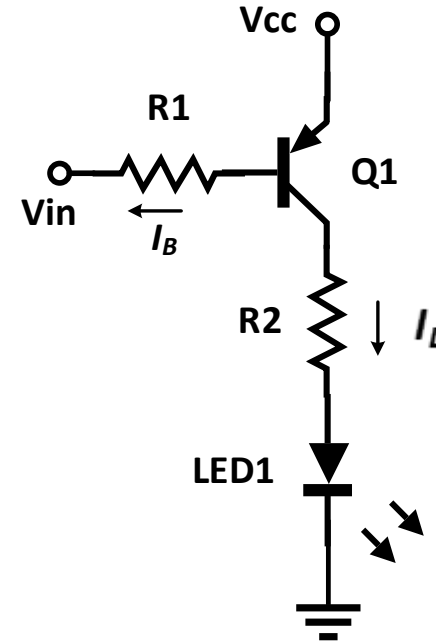
Let  $R_2 = 270\ \Omega$ ,  $\Rightarrow I_L = 10.3\text{ mA}$ .

$$I_B = [(V_{in})_{\text{high}} - V_{BES} - 0] / R_1 > I_L / \beta_{\text{min}}$$

$$\Rightarrow (5 - 0.8 - 0) / R_1 > 10.3 / 50 \Rightarrow R_1 < 20.38\text{ k}\Omega.$$

Let  $R_1 = 18\text{ k}\Omega$ .

**PNP  
Switch for  
Load  
Connected  
to -ve  
Supply End**



$V_{CC} = 5\text{ V}$ .  $V_{in} : 0$  (LED on),  $5\text{ V}$  (LED off).  $\beta > 50$ .  
 $I_L$  for full brightness =  $10\text{ mA}$ . LED drop =  $2\text{ V}$ .

$$I_L = [V_{CC} - V_{ECS} - V_{LED}] / R_2 = [5 - 0.2 - 2] / R_2 > 10\text{ mA}$$

$$\Rightarrow R_2 < 2.8 / 10\text{ k}\Omega = 280\ \Omega.$$

Let  $R_2 = 270\ \Omega$ ,  $\Rightarrow I_L = 10.3\text{ mA}$ .

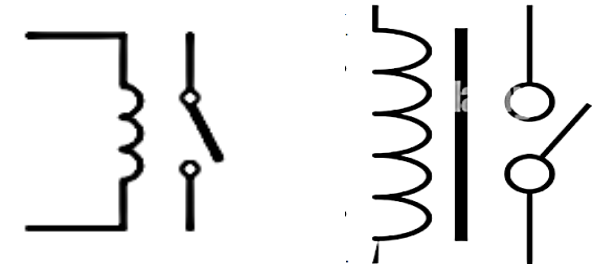
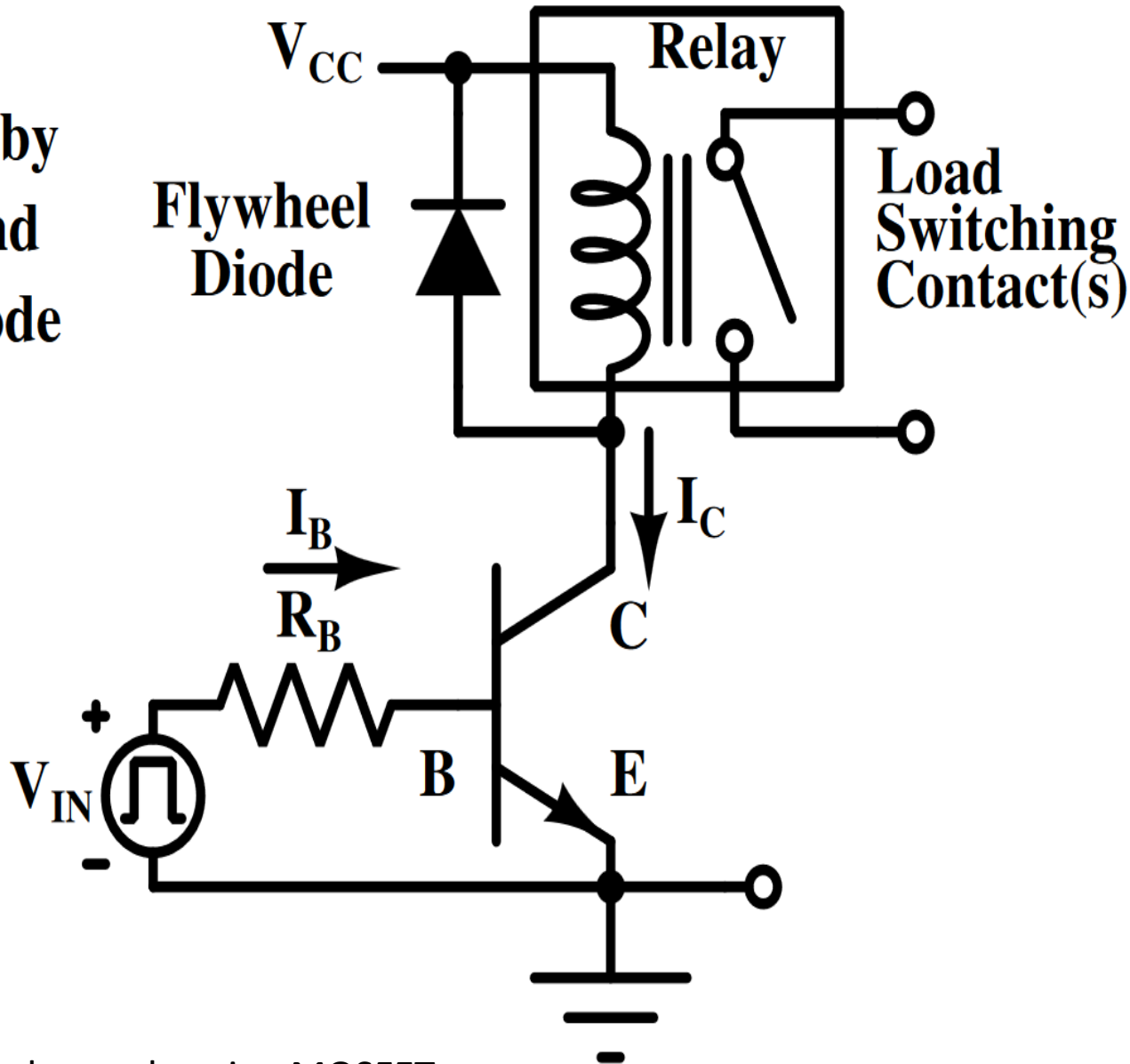
$$I_B = [V_{CC} - V_{EBS} - (V_{in})_{\text{low}}] / R_1 > I_L / \beta_{\text{min}}$$

$$\Rightarrow (5 - 0.8 - 0) / R_1 > 10.3 / 50 \Rightarrow R_1 < 20.38\text{ k}\Omega.$$

Let  $R_1 = 18\text{ k}\Omega$ .

# Relay Operation Using a BJT Switch

$R_L$  replaced by  
Relay coil and  
Flywheel diode

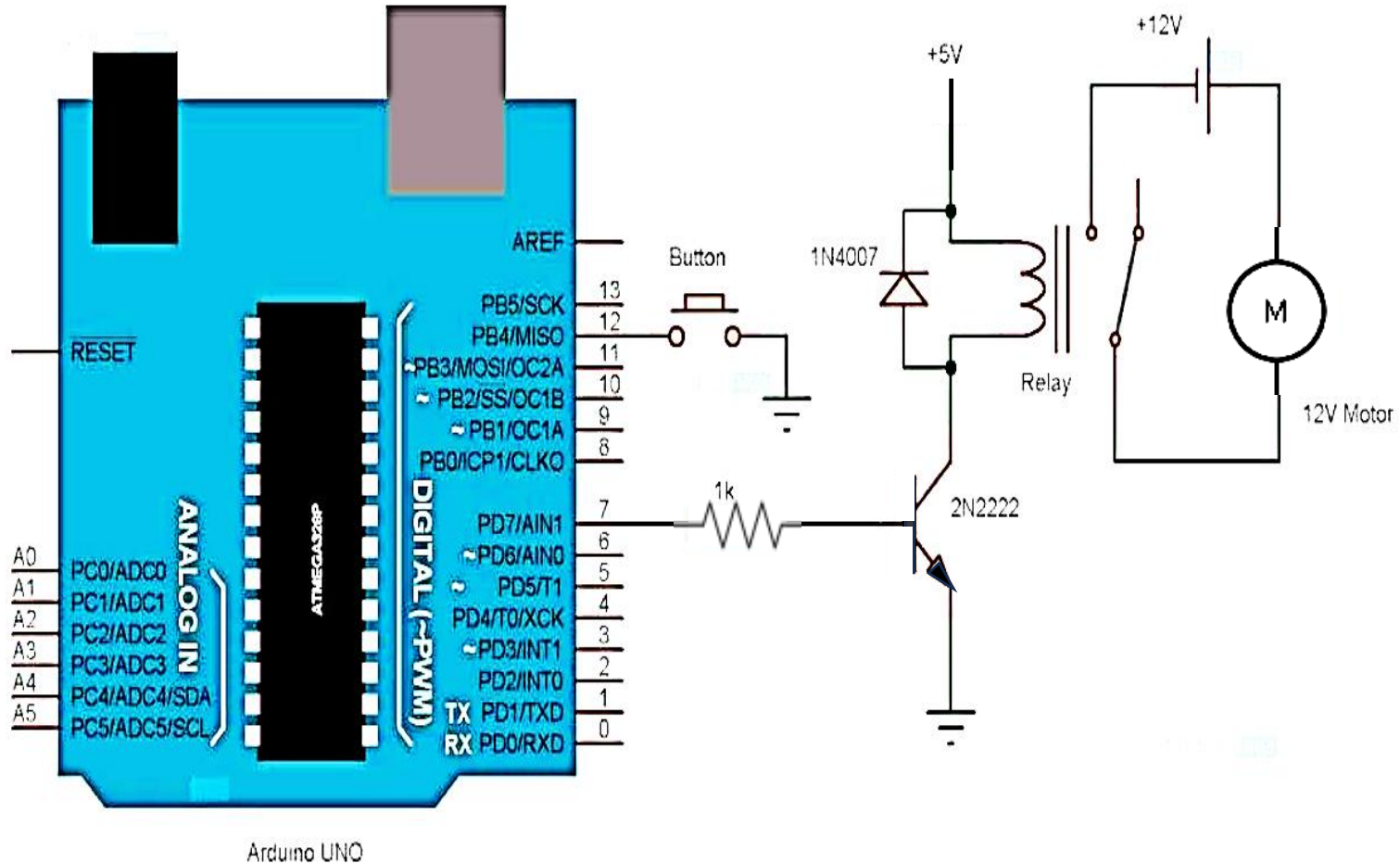


Circuit Symbols for a Relay

By controlling base current ( $I_B$ ) of BJT, high relay coil current ( $= I_C$ ) can be switched.

Current Gain:  $\beta = I_C / I_B$

# Relay Switching Using Micro-Controller (Arduino)



Arduino Relay Control Circuit Diagram

Source: <https://www.electronicshub.org/arduino-relay-control/>

## Example

Control of a relay with 'Arduino' digital output pin ( PD7) and NPN transistor (2N2222).

Relay coil current = 60 mA.  
 Transistor  $\beta_{\min} = 30$ .

Set the pin PD7 to 'Hi'. It will put the transistor in ON state, allowing current to flow through the relay coil making the relay ON.

$$I_B > \text{Relay current} / \beta_{\min} = 2 \text{ mA.}$$

Diode connected in parallel with the relay avoids sudden change of current in the relay coil.



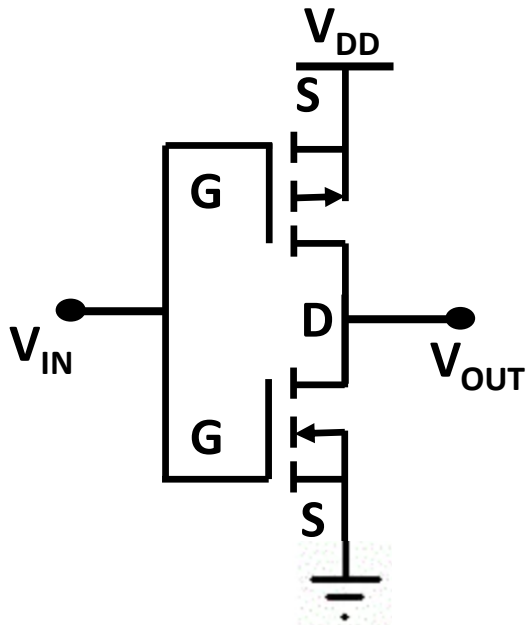
# Some Logic Gates using MOSFETs

- CMOS Inverter
- CMOS NAND Gate – Universal gate
- CMOS NOR Gate – Universal Gate
- CMOS Tri-State Inverter

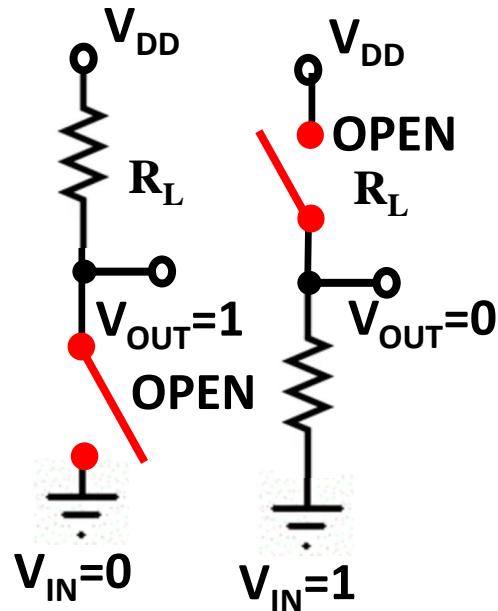
## Complementary Metal Oxide Semiconductor Circuits

1. Combination of NMOS and PMOS Transistors
2. Usually same gate signal goes to NMOS and its complementary PMOS transistors for logic circuits
3. Negligible steady-state power consumption in CMOS digital circuits

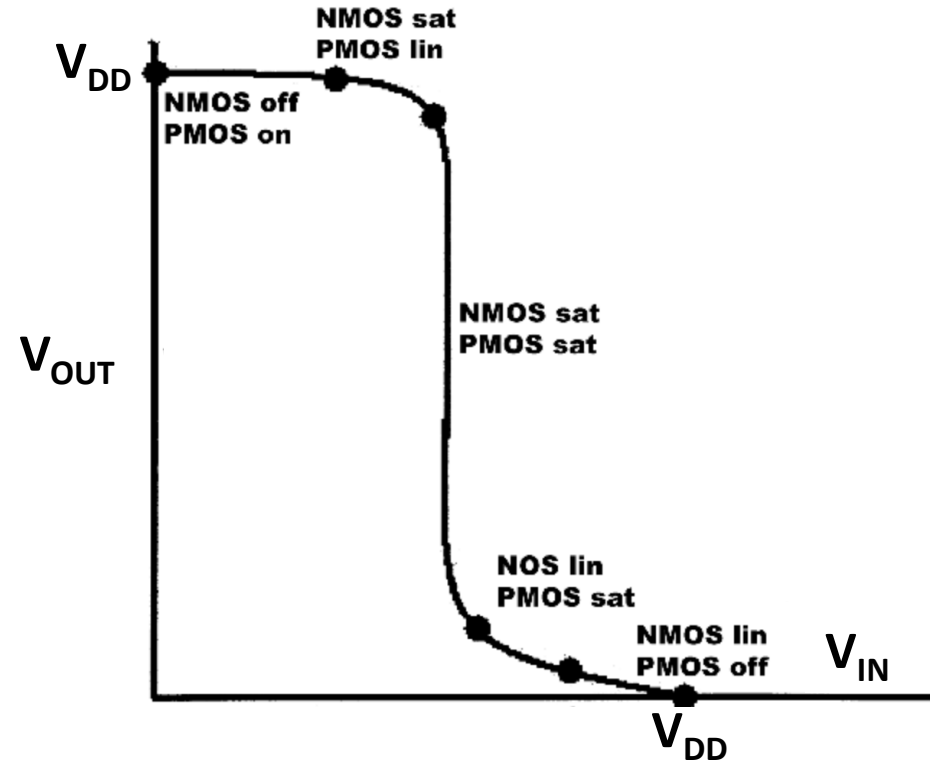
# CMOS Inverter



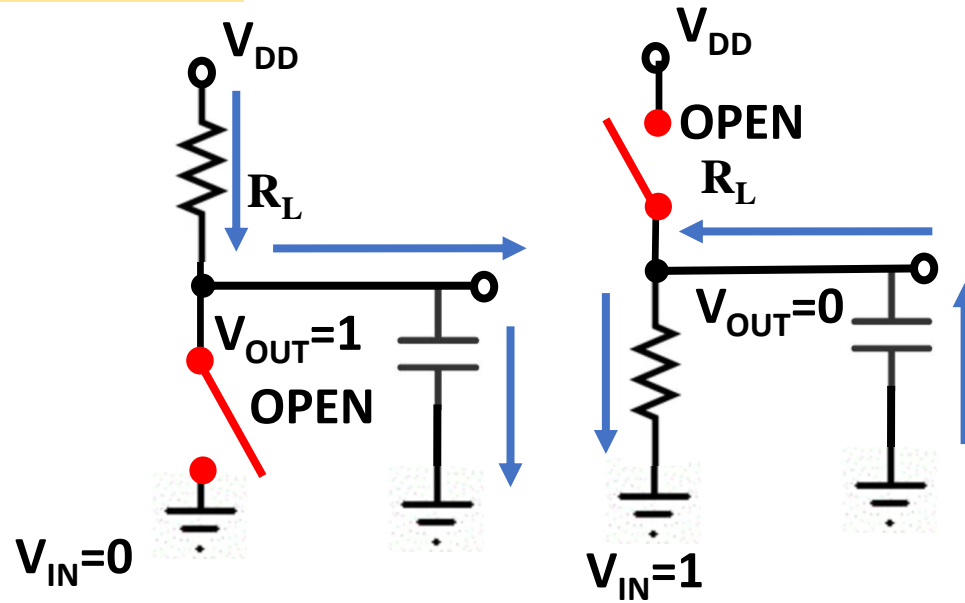
Schematic of a CMOS Inverter



Ideal Digital Operation



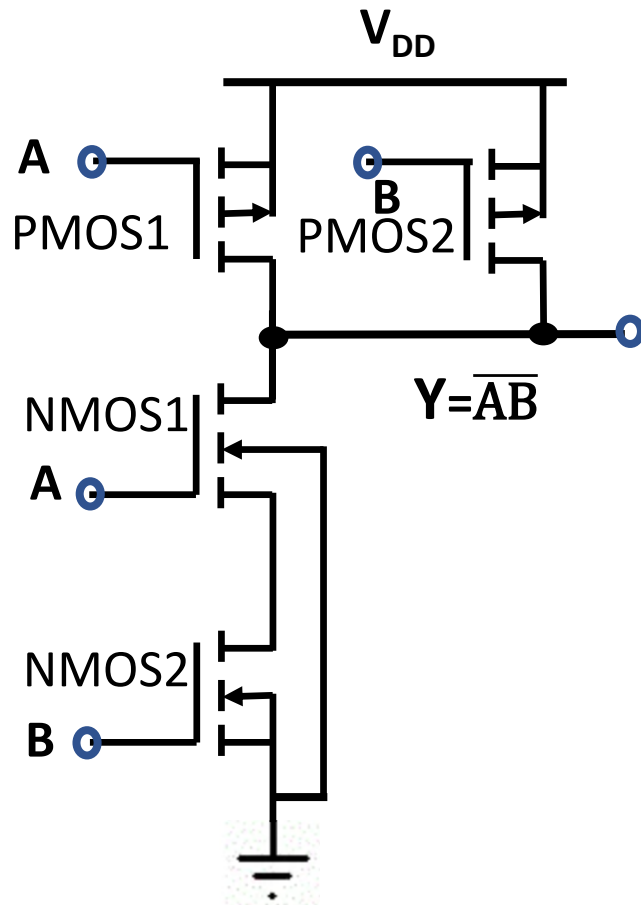
Practical Inverter Characteristics



Origin of delay in an inverter

1. Turn-ON delay – Output low to high
2. Turn-OFF delay – Output high to low

# CMOS 2-INPUT NAND Gate

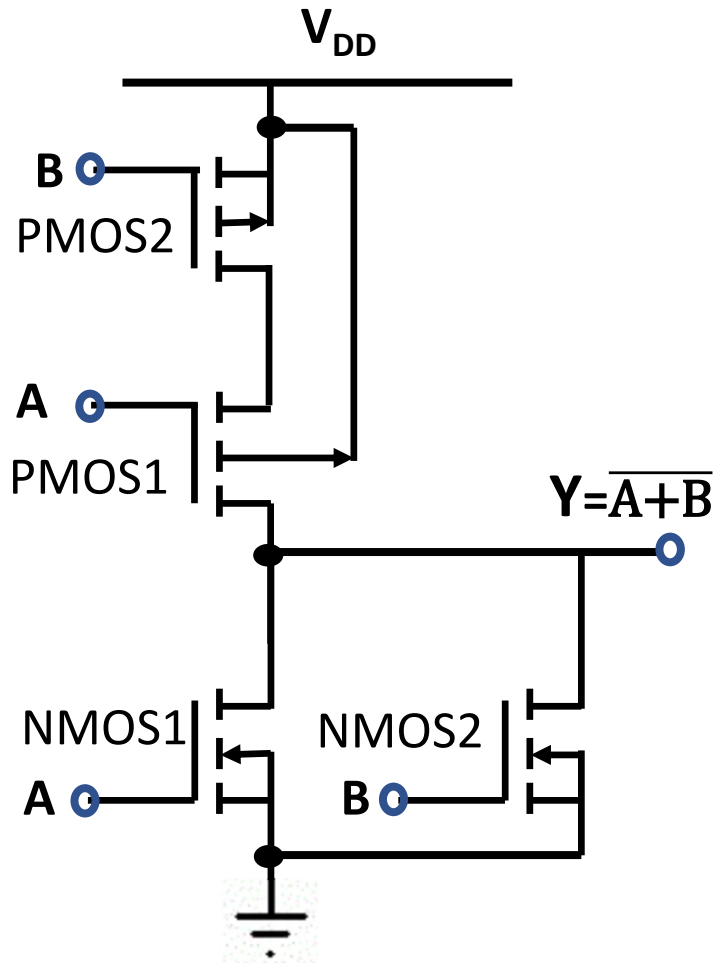


TRUTH TABLE

A	B	Y	NMOS1	PMOS1	NMOS2	PMOS2
0	0	1	OFF	ON	OFF	ON
0	1	1	OFF	ON	ON	OFF
1	0	1	ON	OFF	OFF	ON
1	1	0	ON	OFF	ON	OFF

STATE OF THE TRANSISTORS

# CMOS 2-INPUT NOR Gate

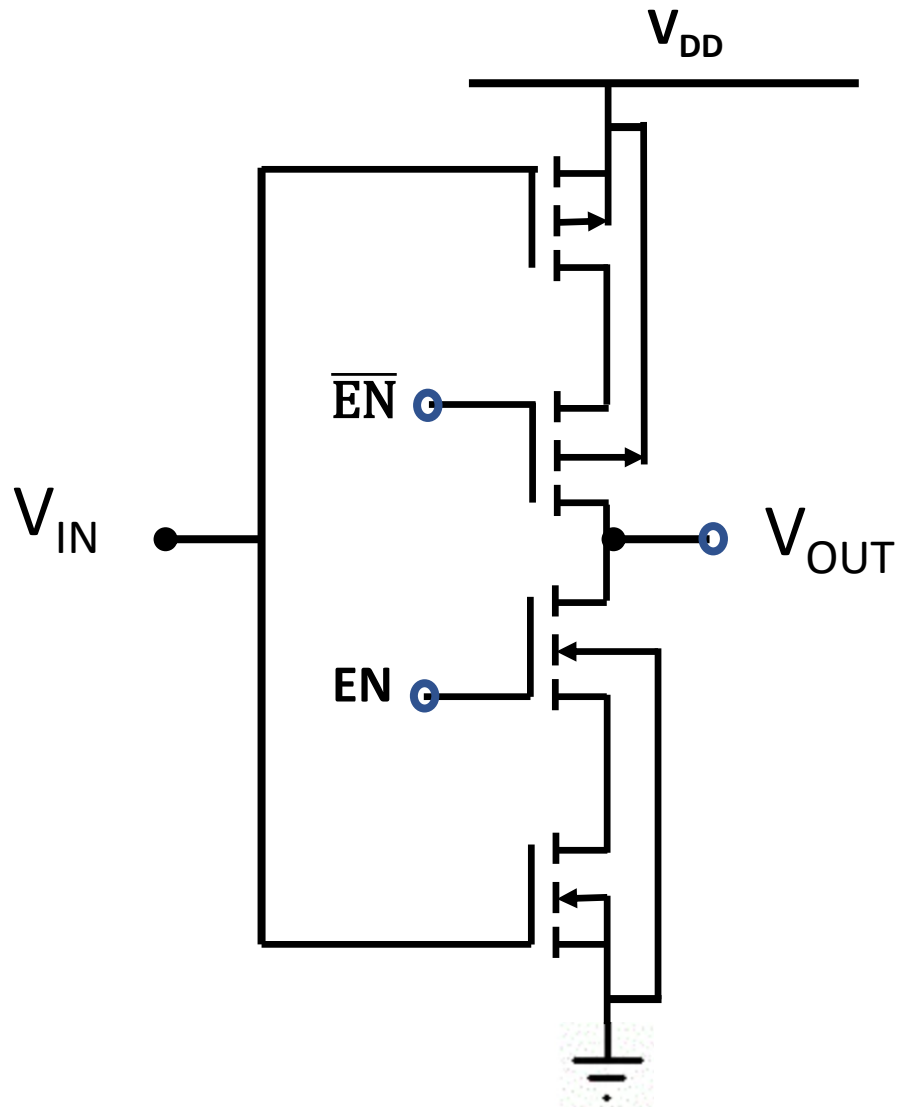


TRUTH TABLE

A	B	Y	NMOS1	PMOS1	NMOS2	PMOS2
0	0	1	OFF	ON	OFF	ON
0	1	0	OFF	ON	ON	OFF
1	0	0	ON	OFF	OFF	ON
1	1	0	ON	OFF	ON	OFF

STATE OF THE TRANSISTORS

# CMOS Tri-State Inverter



- When  $EN=1$ ,  $V_{OUT} = \overline{V_{IN}}$
- When  $EN=0$ ,  $V_{OUT}$  is in the high impedance state

# Questions and Discussions